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CIRCUIT ANALYSIS USING THE  
DRIVING-POINT-IMPEDANCE TECHNIQUE

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### Abstract

This report presents a useful electronic circuit analysis and design technique which was developed at the University of New Mexico by Dr. R. D. Kelly.

## Acknowledgment

The technique presented in this paper was developed by Dr. R. D. Kelly, Professor of Electrical Engineering at the University of New Mexico. The author wishes to thank Dr. Kelly for his permission to present this material.

The blank pages in this report have been included to provide space for making notes. The report should be placed in a loose leaf notebook for most effective use.

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# CIRCUIT ANALYSIS USING THE DRIVING-POINT-IMPEDANCE TECHNIQUE

## Introduction

This report presents a useful electronic circuit analysis and design technique which was developed at the University of New Mexico by Dr. R. D. Kelly, Professor of Electrical Engineering. It was written to satisfy the requests made by those Sandia Laboratories personnel who have been informally introduced to this technique and who have expressed the desire for a document of this type. It is the opinion of the author that this technique, known as Driving-Point-Impedance (DPI) Analysis, provides a far greater insight into electronic circuit operation than the more conventional loop, node, or signal flow graph analysis techniques. Once mastered, DPI analysis can be applied to a wide variety of electronic circuits, and quite frequently solutions to circuit problems can be written by inspection in a single step. Successful mastery of this technique requires a thorough knowledge of a few basic circuit theorems and manipulation of a simple set of useful equations for each active device considered, i. e., bipolar transistors, FET's, and vacuum tubes. In general, DPI analysis does not require that a circuit be redrawn with the active devices replaced by their linear models. Anyone who has taken a course in basic transistor circuit analysis is aware of the myriad number of equivalent circuits presented in such a course. The standard approach uses the various hybrid equivalent circuits, i. e., hybrid common emitter, common collector, and common base models, to obtain the desired circuit solutions. In addition to utilizing different transistor models in the analysis, it is quite common to make many simplifying assumptions beyond those already made for the active device models. Quite frequently, the end result of this approach is confusion on the part of the student. It is not uncommon to find circuit designers applying simplified transfer function equations to circuit designs while ignoring many of the original assumptions made during the derivation of these equations; naturally, the predicted circuit response may differ significantly from the actual response. In addition, the use of many different active device models involves many different parameters, some of which are certain to be missing from data sheets. The DPI approach simplifies the writing of transfer functions and requires only a single active device model for all transistor circuits.

Efficient application of DPI analysis to the solution of electronic circuits dictates that the writing of current and voltage divider equations, along with use of the Superposition Theorem, become almost automatic processes. Because of its importance, this material will be covered in the main body of the report, although individuals familiar with these basic concepts may desire to omit it. In order to keep the mathematics from obscuring the analysis technique, circuit solutions have been limited to dc or the sinusoidal steady state. Those familiar with the application of the Laplace transform method can use it along with DPI analysis to solve transient circuit problems;

examples are given in Appendix C. Generally, all-resistive-type networks will be analyzed in order to demonstrate the desired points; however, DPI analysis can be utilized for other types of networks.

## Development of Voltage Divider Equations

Figure 1 illustrates a simple two-resistor voltage divider.

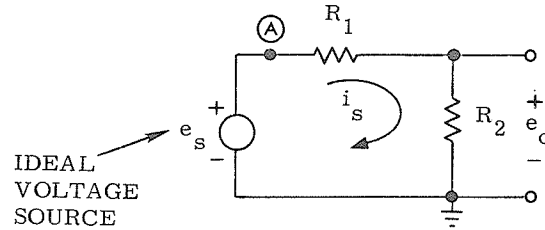


Figure 1. Simple Resistive Voltage Divider

Using Ohm's Law to solve for  $e_o$  in terms of  $e_s$ ,  $R_1$  and  $R_2$ , we have

$$e_o = i_s R_2 , \quad (1)$$

$$i_s = \frac{e_s}{R_1 + R_2} . \quad (2)$$

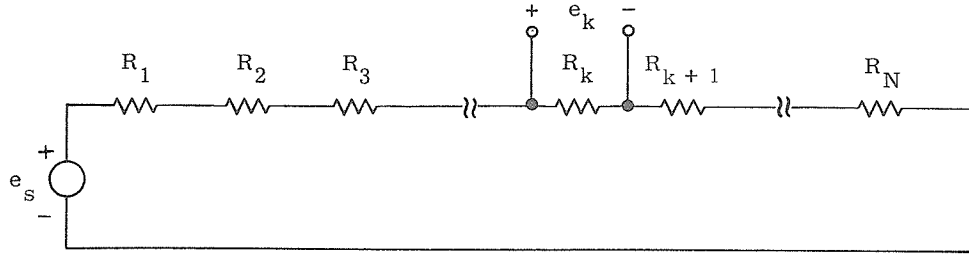
Substituting Equation (2) into (1), we have

$$e_o = e_s \left( \frac{R_2}{R_1 + R_2} \right) . \quad (3)$$

Equation (3) is referred to as a voltage divider equation. It should be clear that Equation (3) can be written in a single step once the pattern is recognized. Likewise, the voltage drop across  $R_1$  using point A as the positive reference terminal is

$$e_{R_1} = e_s \left( \frac{R_1}{R_1 + R_2} \right) .$$

Figure 2 shows a generalized voltage divider circuit along with the voltage divider equation for the voltage drop across resistor  $R_k$ .



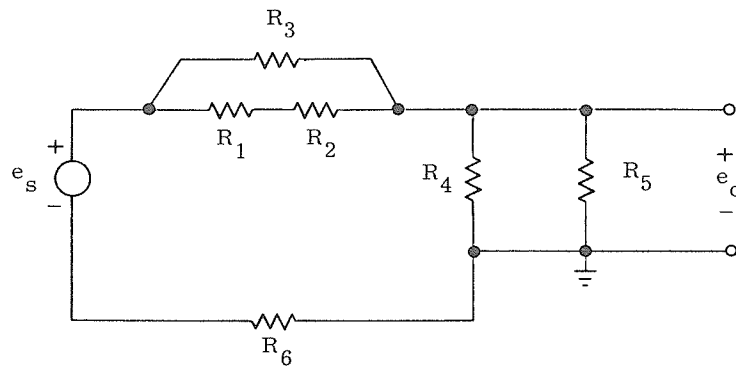
$$e_k = e_s \left( \frac{R_k}{R_1 + R_2 + \dots + R_N} \right) = e_s \left( \frac{R_k}{\sum_{i=1}^N R_i} \right) \quad (4)$$

Figure 2. A Generalized Voltage Divider

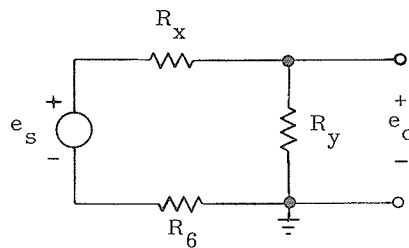
Note especially that any of the  $R_i$  shown in Figure 2 may be a combination of other resistors. This point is demonstrated in the following example.

#### Example 1

Problem--Derive an expression for  $e_o$  in terms of  $e_s$  and the resistors shown using the voltage divider equation (Equation 4).



Solution--We observe that this circuit can be reduced to the series combination of three resistors,





where  $R_x$  is  $R_3$  in parallel with the series combination of  $R_1$  and  $R_2$ , and  $R_y$  is the parallel combination of  $R_4$  and  $R_5$ . Using Equation (4), we have

$$e_o = e_s \left( \frac{R_y}{R_x + R_y + R_6} \right), \quad (5)$$

where

$$R_x = \frac{R_3(R_1 + R_2)}{R_3 + (R_1 + R_2)} \text{ and } R_y = \frac{R_4 R_5}{R_4 + R_5}.$$

Substituting for  $R_x$  and  $R_y$  in Equation (5) yields

$$e_o = e_s \left[ \frac{\left( \frac{R_4 R_5}{R_4 + R_5} \right)}{\left( \frac{R_3 [R_1 + R_2]}{R_3 + [R_1 + R_2]} \right) + \left( \frac{R_4 R_5}{R_4 + R_5} \right) + R_6} \right]. \quad (6)$$

Equations such as (6) can become cumbersome if more than a few resistors are contained in the network, so we introduce a shorthand notation for the parallel combination of two or more resistors. From this point on,  $R_i$  in parallel with  $R_j$  will be written as  $R_i \parallel R_j$  instead of

$\frac{R_i R_j}{R_i + R_j}$  and  $R = R_1 \parallel R_2 \parallel R_3 \parallel \dots \parallel R_N$  will be interpreted to mean

$$R = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \dots + \frac{1}{R_N}}$$

By using this notation for parallel resistors, one can write Equation (6) as

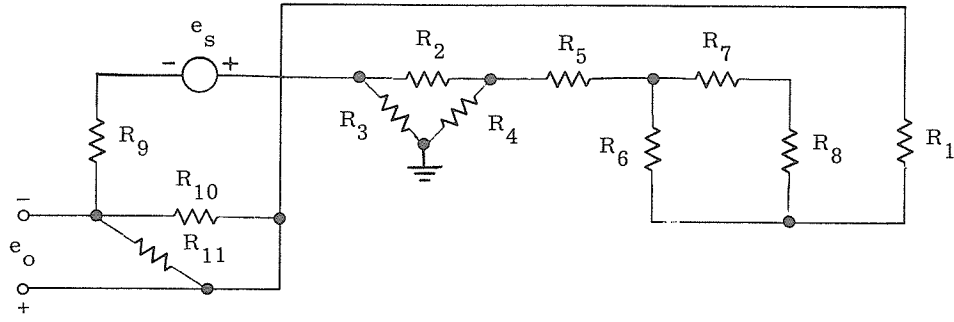
$$e_o = e_s \left[ \frac{(R_4 \parallel R_5)}{(R_4 \parallel R_5) + (R_3 \parallel [R_1 + R_2]) + R_6} \right]. \quad (7)$$

Equation (7) has the form of a voltage divider equation and can be written in a single step directly from the original circuit diagram.

From this point on, all voltage divider equations will be written in the form of Equation (7).

### Example 2

Problem--Using the following circuit, derive an expression for  $e_o$  in a single step. The expression must be in the form of a voltage divider equation.



Solution--

$$e_o = e_s \left[ \frac{(R_{10} \parallel R_{11})}{(R_2 \parallel [R_3 + R_4]) + R_5 + (R_6 \parallel [R_7 + R_8]) + R_1 + (R_{10} \parallel R_{11}) + R_9} \right] .$$

### Development of Current Divider Equations

Figure 3 illustrates a simple two-resistor current divider.

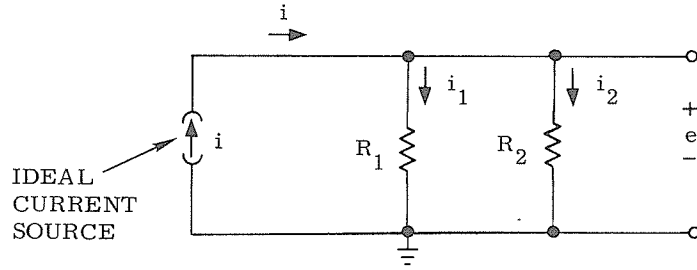


Figure 3. Simple Current Divider

Using Ohm's Law to solve for  $i_1$ , we have

$$i_1 = \frac{e}{R_1} . \quad (8)$$

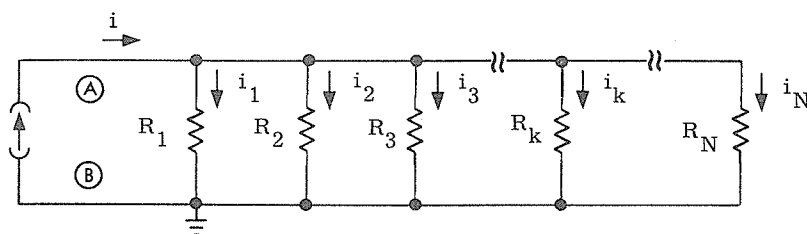
and

$$e = i(R_1 \parallel R_2) . \quad (9)$$

Substituting Equation (9) into (8) and replacing  $R_1 \parallel R_2$  by  $\frac{R_1 R_2}{R_1 + R_2}$ , we have

$$i_1 = \frac{i(R_1 \parallel R_2)}{R_1} = \frac{i}{R_1} \left( \frac{R_1 R_2}{R_1 + R_2} \right) = i \left( \frac{R_2}{R_1 + R_2} \right) . \quad (10)$$

Equation (10) is referred to as a current divider equation. Equation (10) has a form similar to the voltage divider equation; but note that in the solution for  $i_1$ , which is the portion of  $i$  passing through  $R_1$ ,  $R_2$  is used in the divider fraction. Thus, the divider fraction uses the resistor opposite the one in which the current is to be determined. Figure 4 shows a generalized current divider circuit along with the equation for the current through resistor  $R_k$ .



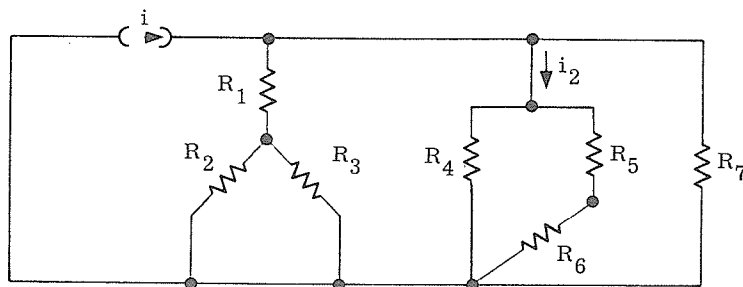
$$i_k = i \left[ \frac{(R_1 || R_2 || R_3 || \dots || R_{k-1} || R_{k+1} || \dots || R_N)}{(R_1 || R_2 || R_3 || \dots || R_{k-1} || R_{k+1} || \dots || R_N) + R_k} \right] \quad (11)$$

Figure 4. A Generalized Current Divider

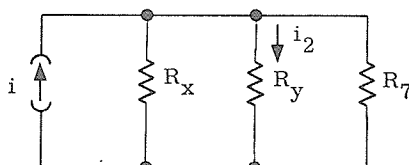
Any of the  $R_i$  shown in Figure 4 can be a combination of other resistors which are connected between points (A) and (B).

### Example 3

Problem--Derive an expression for  $i_2$  in terms of  $i$  and the resistors shown and express the answer in the form of the current divider equation (Equation 11).



Solution--We observe that this circuit can be reduced to the parallel combination of three resistors,



where  $R_x$  is  $R_1$  in series with the parallel combination of  $R_2$  and  $R_3$ , and  $R_y$  is  $R_4$  in parallel with the series combination of  $R_5$  and  $R_6$ .

Using Equation (11), we have

$$i_2 = i \left( \frac{[R_x || R_7]}{[R_x || R_7] + R_y} \right) \quad (12)$$

where

$$R_x = (R_1 + [R_2 || R_3]) \text{ and } R_y = (R_4 || [R_5 + R_6])$$

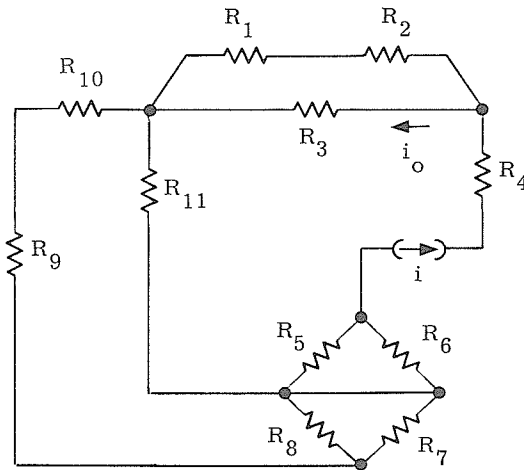
Substituting for  $R_x$  and  $R_y$  in Equation (12), we have

$$i_2 = i \left[ \frac{(R_1 + [R_2 || R_3]) || R_7}{\{(R_1 + [R_2 || R_3]) || R_7\} + (R_4 || [R_5 + R_6])} \right] \quad (13)$$

Equation (13) can be written in a single step. The intermediate steps are included only to clarify the reasoning process.

#### Example 4

Problem--Derive an expression for  $i_o$  in a single step. The expression must be in the form of a current divider equation.



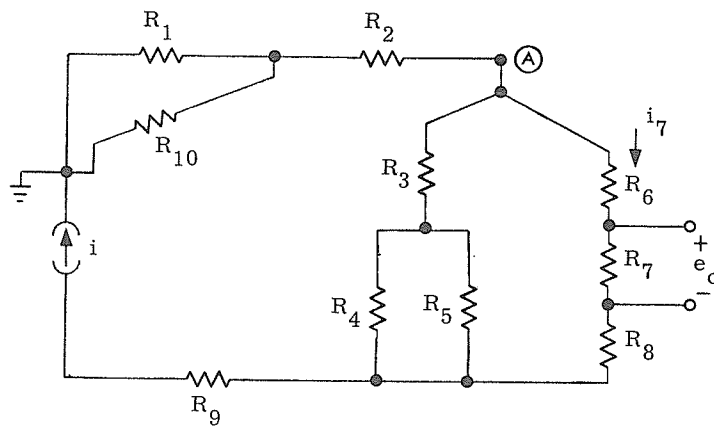
Solution--

$$i_o = i \left( \frac{[R_1 + R_2]}{[R_1 + R_2] + R_3} \right) \quad (14)$$

The following examples will use voltage and current divider equations to obtain the desired solution. Additional steps will be included in order to demonstrate the reasoning process involved in obtaining the answer, but it is emphasized that the answer can and should be written in a single step. A facility for writing the answers in a single step must be gained in order to take full advantage of DPI analysis.

### Example 5

Problem--From the circuit below determine  $e_o$  as a function of  $i$  and the resistors using current divider equations. Write the answer in a single step.



Solution--Using a current divider equation and Ohm's Law, we obtain the solution

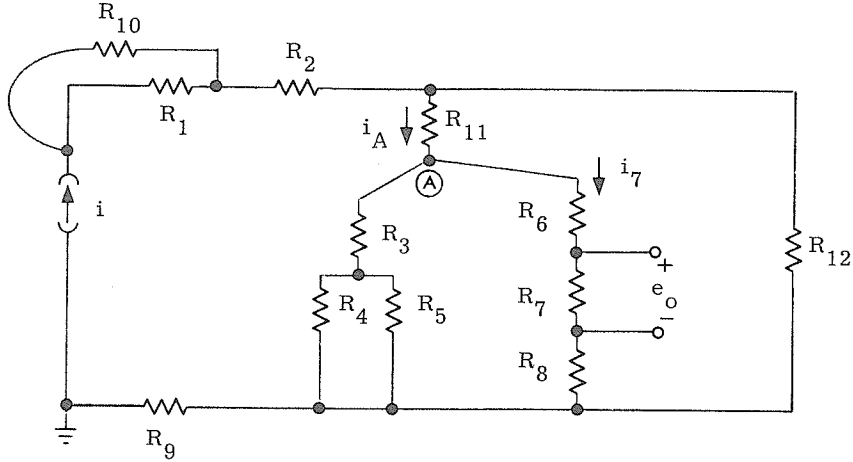
$$e_o = i \underbrace{\left[ \frac{(R_3 + [R_4 || R_5])}{(R_3 + [R_4 || R_5]) + (R_6 + R_7 + R_8)} \right]}_{i_7} R_7 \quad (15)$$

Note especially that the ground connected to the upper end of the current source has no effect. The reasoning is as follows. To find  $e_o$ , we must find the current through  $R_7$ . When the current through  $R_7$  is known, the voltage across  $R_7$  is  $i_7 R_7$ . Note that the current entering node (A) is  $i$ . If this is not obvious, note that the total current  $i$  must flow through  $R_9$ , but if it does, it must enter at node (A) because that is its only possible path. Knowing the current entering node (A) permits us to write the current divider equation to find  $i_7$ . The  $i_7 R_7$  product yields  $e_o$ . Resistors  $R_1$ ,  $R_2$ ,  $R_9$ , and  $R_{10}$  do not enter into the equation because they have no effect on the current divider of interest.

Quite frequently, multiple current dividers occur in a single circuit. Example 6 demonstrates how to handle a multiple current divider.

### Example 6

Problem--Determine  $e_o$  as a function of  $i$  and the resistors using current divider equations. Write the answer in a single step.



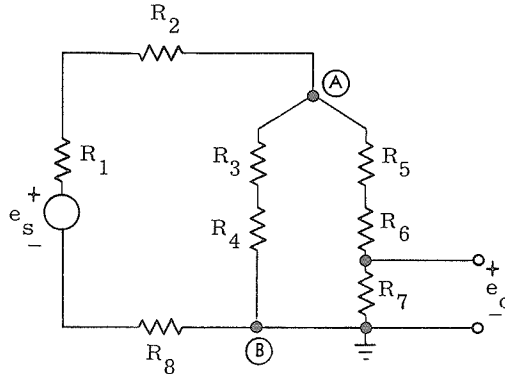
Solution--

$$e_o = i \underbrace{\left[ \frac{R_{12}}{R_{12} + \left[ R_{11} + \left\{ \left( R_3 + [R_4 || R_5] \right) || (R_6 + R_7 + R_8) \right\} \right]} \right]}_{i_A} \underbrace{\left[ \frac{(R_3 + [R_4 || R_5])}{(R_3 + [R_4 || R_5]) + (R_6 + R_7 + R_8)} \right]}_{i_7} R_7 \quad (16)$$

To find  $i_7$ , the portion of  $i$  which flows through  $R_7$ , we must write two current divider fractions. Parentheses, braces, and brackets are used liberally in order to clarify the equations.

### Example 7

Problem--Determine  $e_o$  as a function of  $e_s$  and the resistors using voltage divider equations. Write the solution in a single step.



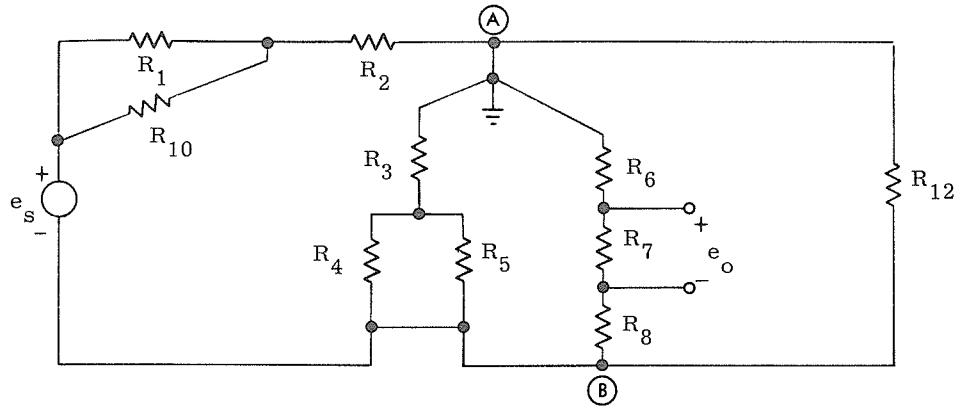
Solution--

$$e_o = e_s \underbrace{\left[ \frac{([R_3 + R_4] \parallel [R_5 + R_6 + R_7])}{R_1 + R_2 + ([R_3 + R_4] \parallel [R_5 + R_6 + R_7]) + R_8} \right]}_{V_{AB}} \left[ \frac{R_7}{R_5 + R_6 + R_7} \right] \quad (17)$$

First, the fraction of  $e_s$  appearing between nodes (A) and (B) is found; then the portion of this voltage ( $V_{AB}$ ) appearing across  $R_7$  is determined. This amounts to writing a double voltage divider equation.

#### Example 8

Problem--Determine  $e_o$  as a function of  $e_s$  and the resistors using voltage divider equations. Write the solution in a single step.



Solution--

$$e_o = e_s \underbrace{\left[ \frac{[(R_{12}) \parallel (R_3 + \{R_4 \parallel R_5\}) \parallel (R_6 + R_7 + R_8)]}{[(R_{12}) \parallel (R_3 + \{R_4 \parallel R_5\}) \parallel (R_6 + R_7 + R_8)] + R_2 + (R_1 \parallel R_{10})} \right]}_{V_{AB}} \left[ \frac{R_7}{R_6 + R_7 + R_8} \right] \quad (18)$$

## Superposition Theorem

DPI analysis frequently requires application of the superposition theorem.<sup>1</sup> This states that the voltage across, or the current through, any element can be computed in the following way: Replace all the independent generators except one by their internal impedances and compute the voltage across (or the current through) the element in question. Repeat this procedure for each independent generator in turn. Then, find the algebraic sum of all the calculated voltages across (or the currents through) the element in question; this will be the actual voltage across (or the current through) the element. Note especially that the generators that are replaced by their internal impedances are independent generators. An independent generator is one whose output is independent of any voltage or current in the circuit connected to the generator. When electronic circuits containing linear models of the active devices, e.g., bipolar transistors, FET's, etc., are analyzed, it is common practice to redraw the circuits, replacing the active devices with their associated linear equivalent circuits. Consider the common emitter hybrid equivalent circuit of an NPN transistor (Figure 5).

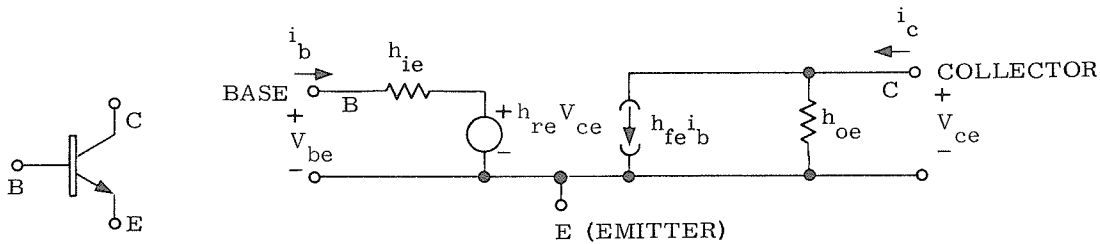


Figure 5. Hybrid Model of NPN Transistor Connected in Common-Emitter Configuration

This model contains a current-controlled current source and a voltage-controlled voltage source. The current source  $h_{fe} i_b$  is controlled by the  $i_b$  current, and the voltage source  $h_{re} V_{ce}$  is controlled by the  $V_{ce}$  voltage. Both of these sources are referred to as dependent generators because their outputs are dependent functions of a voltage or current which exists elsewhere in the circuit. If the superposition theorem is applied to such a circuit, these dependent generators are not replaced by their internal impedances but are retained throughout the analysis.

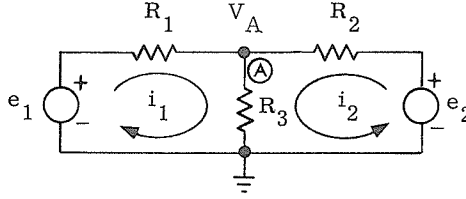
Only series parallel type networks will be investigated in the examples given in this section. Other types of networks which are not easily classified will be discussed in a later section.

Example 9 demonstrates the advantages of using the superposition theorem as opposed to loop or node analysis.



Example 9

Problem-- Determine  $V_A$  by using loop and node analysis and then by application of the superposition theorem; prove that the answers are the same by letting  $R_1 = R_2 = R_3 = 1\Omega$ , and  $e_1 = e_2 = 1\text{ V}$ .



Loop Analysis--Assume loop currents  $i_1$  and  $i_2$  flow as indicated. Using Kirchhoff's voltage law (KVL), we sum the voltages around each loop.

$$i_1(R_1 + R_3) + i_2 R_3 = e_1 \quad (19)$$

$$i_1 R_3 + i_2(R_2 + R_3) = e_2 \quad (20)$$

Equations (19) and (20) can be solved simultaneously for  $i_1$  and  $i_2$ ; then  $V_A$  is found to be

$$V_A = (i_1 + i_2) R_3$$

Node Analysis--Using Kirchhoff's current law (KCL) to sum the currents entering node (A), we have

$$\frac{e_1 - V_A}{R_1} + \frac{e_2 - V_A}{R_2} = \frac{V_A}{R_3}$$

$$\frac{e_1}{R_1} + \frac{e_2}{R_2} = V_A \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)$$

$$V_A = \left( \frac{\frac{e_1}{R_1} + \frac{e_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \right)$$

Superposition--Using superposition, we can write the answer in a single step by inspection.

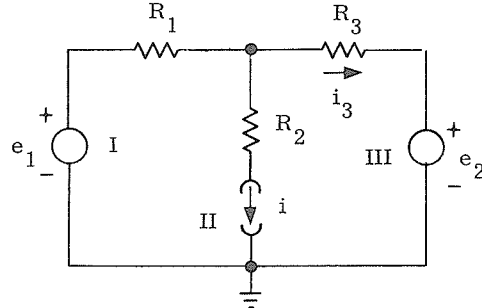
$$V_A = e_1 \underbrace{\left( \frac{[R_3 \parallel R_2]}{[R_3 \parallel R_2] + R_1} \right)}_{\substack{\text{This part found by} \\ \text{setting } e_2 \text{ to zero} \\ \text{and using the voltage} \\ \text{divider equation.}}} + e_2 \underbrace{\left( \frac{[R_1 \parallel R_3]}{[R_1 \parallel R_3] + R_2} \right)}_{\substack{\text{This part found by} \\ \text{setting } e_1 \text{ to zero} \\ \text{and using the voltage} \\ \text{divider equation.}}} \quad (21)$$

Substituting the given values for resistance and voltage into the equations will prove the answers are the same, i. e.,  $V_A = 2/3 \text{ V}$ .

The next example demonstrates the application of the superposition theorem to a circuit containing mixed sources.

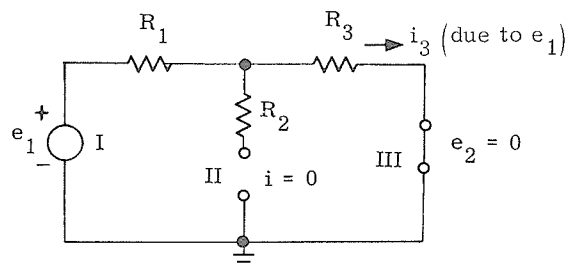
#### Example 10

Problem--Determine current  $i_3$  by application of the superposition theorem.



Solution--This circuit contains three independent generators; therefore, the contribution made to  $i_3$  by each generator can be found and the sum of these individual currents will yield the resultant current  $i_3$ .

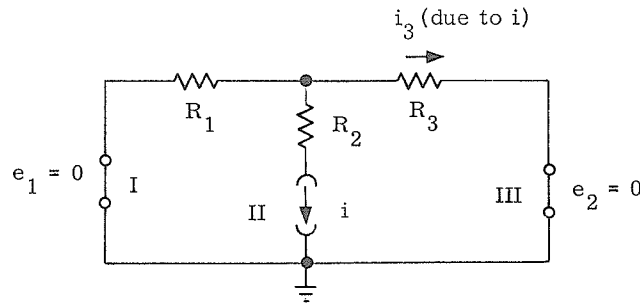
Step 1 -- Replace independent generators II and III by their internal impedances and determine the portion and direction of  $i_3$  due to  $e_1$  acting alone.



$$i_3 \text{ (due to } e_1) = \left( \frac{e_1}{R_1 + R_3} \right) \quad (22)$$

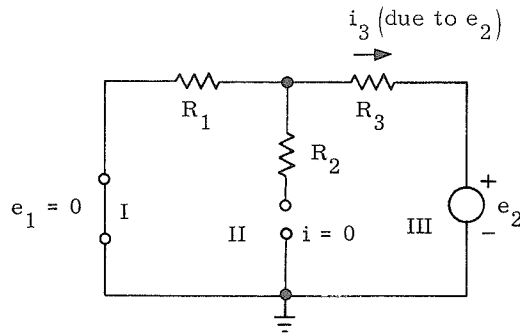
Note especially that an ideal independent current source is replaced by an infinite impedance (open circuit) and an ideal independent voltage source is replaced by zero impedance (short circuit).

Step 2--Replace independent generators I and III by their internal impedances and determine the portion and direction of  $i_3$  due to  $i$  acting alone.



$$i_3 \text{ (due to } i) = -i \left( \frac{R_1}{R_1 + R_3} \right) \quad \text{(current divider form)} \quad (23)$$

Step 3--Replace independent generators I and II by their internal impedances and determine the portion and direction of  $i_3$  due to  $e_2$  acting alone.



$$i_3 \text{ (due to } e_2) = - \left( \frac{e_2}{R_1 + R_3} \right) \quad (24)$$

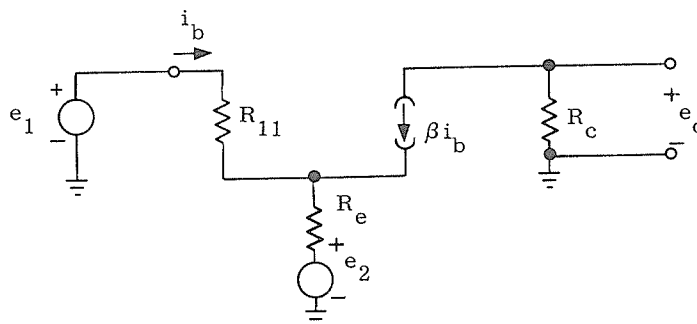
Step 4--The value of  $i_3$  is given by the algebraic sum of Equations (22), (23), and (24).

$$i_3 = \left( \frac{e_1}{R_1 + R_3} \right) - i \left( \frac{R_1}{R_1 + R_3} \right) - \left( \frac{e_2}{R_1 + R_3} \right) \quad (25)$$

Example 11 demonstrates how a dependent source can be handled by the superposition theorem.

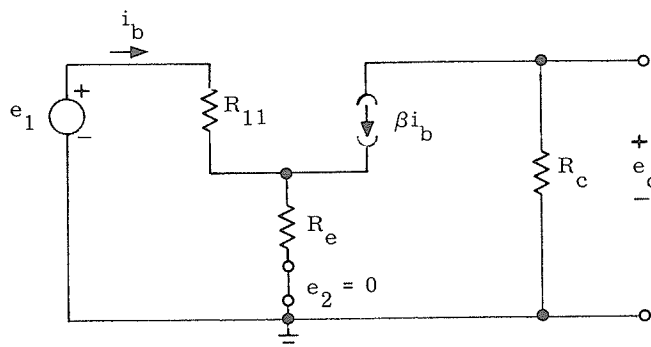
### Example 11

Problem--Determine  $e_o$  as a function of the independent sources  $e_1$  and  $e_2$ .



### Solution--

Step 1--Replace independent generator  $e_2$  by its internal impedance and determine the portion of  $e_o$  due to source  $e_1$  acting alone.



First, we know  $e_o = -\beta i_b R_c$  because all of the current from the dependent  $\beta i_b$  current generator flows through resistor  $R_c$ .

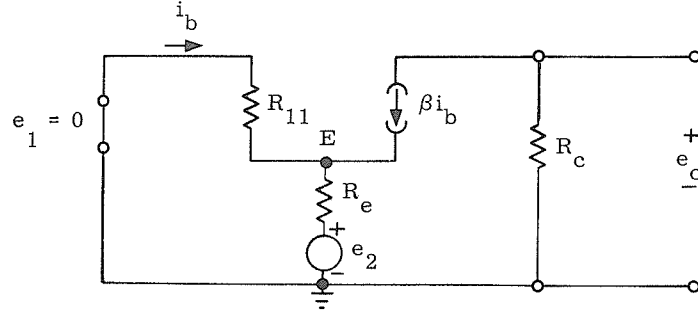
Writing the voltage drops around the  $R_{11}$ ,  $R_e$ ,  $e_2$ ,  $e_1$  loop and solving for  $i_b$ , we have

$$i_b \text{ (due to } e_1) = \left( \frac{e_1}{R_{11} + (1 + \beta) R_e} \right) .$$

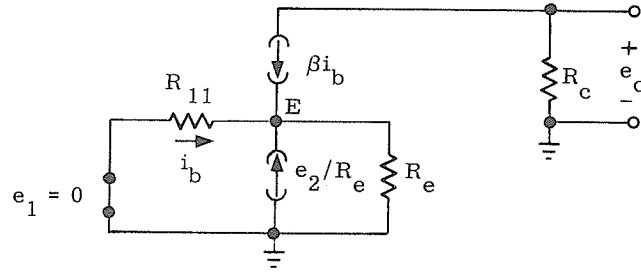
So

$$e_o \text{ (due to } e_1) = - \left( \frac{e_1}{R_{11} + (1 + \beta) R_e} \right) \beta R_c . \quad (26)$$

Step 2--Replace independent generator  $e_1$  by its internal impedance and determine the portion of  $e_o$  due to  $e_2$  acting alone.



This circuit is best handled by replacing the  $R_e, e_2$  combination by its Norton equivalent circuit,\* redrawing the circuit, and solving for  $i_b$ .



Applying the current divider equation at node E, we have

$$i_b = - \left[ \beta i_b + \frac{e_2}{R_e} \right] \left( \frac{R_e}{R_e + R_{11}} \right)$$

Solving for  $i_b$ ,

$$i_b (\text{due to } e_2) = - \left( \frac{e_2}{R_{11} + R_e (1 + \beta)} \right)$$

Now that the value of  $i_b$  due to  $e_2$  is known, we can substitute it into the expression for  $e_o$ .

---

\*Refer to Appendix A for a review of Norton's theorem.

$$\begin{aligned}
 e_o \text{ (due to } e_2) &= -\beta i_b \text{ (due to } e_2) R_c \\
 &= \left[ \frac{e_2}{R_{11} + R_e (1+\beta)} \right] \beta R_c
 \end{aligned} \tag{27}$$

Step 3--The value of  $e_o$  is given by the algebraic sum of Equations (26) and (27).

$$e_o = - \left( \frac{e_1}{R_{11} + (1+\beta)R_e} \right) \beta R_c + \left( \frac{e_2}{R_{11} + (1+\beta)R_e} \right) \beta R_c \tag{28}$$

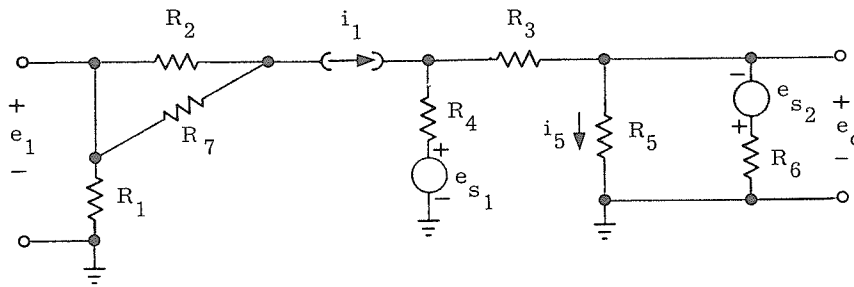
The point to be emphasized in the solution of this circuit by application of the superposition theorem is that the dependent generator is never modified.

Only the independent generators are replaced by their internal impedances.

Generally, the intermediate steps shown in Examples 9, 10, and 11 are omitted and the solutions are written in a single step.

#### Example 12

Problem--Using the superposition theorem, derive expressions for  $i_5$  and  $e_1$  in a single step.



Solution--

$$e_1 = -i_1 R_1 \tag{29}$$

$$i_5 = i_1 \underbrace{\left( \frac{R_4}{R_4 + [R_3 + (R_5 \parallel R_6)]} \right)}_{\text{Dual current divider giving portion of } i_5 \text{ due to } i_1 \text{ source acting alone}} + e_{s1} \underbrace{\left( \frac{[R_5 \parallel R_6]}{[R_5 \parallel R_6] + R_3 + R_4} \right)}_{\text{Voltage divider giving portion of } e_{s1} \text{ acting alone which appears across } R_5, \text{ causing a current through } R_5} \left( \frac{1}{R_5} \right)$$

$$\begin{aligned}
 &-e_{s2} \underbrace{\left( \frac{[R_5 \parallel (R_3 + R_4)]}{[R_5 \parallel (R_3 + R_4)] + R_6} \right)}_{\text{Voltage divider giving portion of } e_{s2} \text{ acting alone which appears across } R_5, \text{ causing a current through } R_5} \left( \frac{1}{R_5} \right)
 \end{aligned} \tag{30}$$

## Driving-Point- Impedance (DPI) Equations

If the driving-point-impedance at each terminal of a bipolar transistor, FET, or vacuum tube (triode or pentode) operating in its linear region is known, the application of the aforementioned techniques will yield solutions to many electronic circuits in a single step. The analysis can be extended to the entire range of operation by utilizing break-point techniques. The expressions for the DPI seen at each terminal of a bipolar transistor, J-FET and (triode or pentode) vacuum tube will now be derived. For the sake of brevity, little will be said about the circuit models except that the implied assumptions made in using these models have proved to be sufficiently accurate for most engineering calculations where internal device capacitances can be ignored.<sup>2</sup>

### Bipolar Transistor DPI Equations

The circuit shown in Figure 6 (A), along with the simplified hybrid model of the transistor in the common-emitter configuration (Figure 6B)<sup>2</sup>, will be used to derive expressions for the DPI seen looking into each terminal of the bipolar transistor.

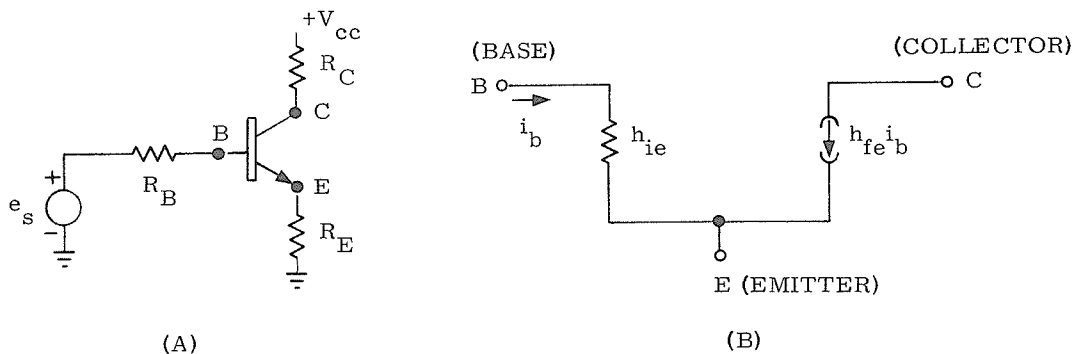


Figure 6. Circuit for Determination of Bipolar Transistor DPI Equations

If the simplified hybrid model of the transistor shown in Figure 6 (B) is compared with the complete hybrid model of Figure 5, it can be seen that the  $h_{oe}$  and  $h_{re}$  parameters have been omitted. In practice these parameters are usually not specified on data sheets. Their inclusion in the hybrid model unduly complicates the circuit analysis and provides no benefits to speak of.  $h_{ie}$  is defined as the dynamic base-to-emitter resistance, and  $h_{fe}$  is defined as the dynamic small signal forward current gain.  $h_{fe}$  is usually referred to as the beta ( $\beta$ ) of the transistor. All of the small signal parameters are defined at the quiescent operating point chosen for the device.

$h_{ie} = \left. \frac{\partial v_{be}}{\partial i_b} \right _{v_{ce} = \text{Constant}}$	$h_{fe} = \left. \frac{\partial i_c}{\partial i_b} \right _{v_{ce} = \text{Constant}}$
Base-to-emitter impedance at quiescent operating point (ohms)	Forward current gain at quiescent operating point (dimensionless)

$h_{ie}$  and  $\beta$  are the only two parameters that will be used in the analysis of transistor circuits using the DPI technique, as opposed to the more conventional approach of using common-emitter, common-collector, and common-base hybrid parameters. Although  $h_{ie}$  can be measured on a curve tracer, a useful formula for determining  $h_{ie}$  at room temperature is given by Equation (31).<sup>3</sup>

$$h_{ie} \approx \frac{26 \times 10^{-3} (1 + \beta)}{I_{EQ}} \quad (31)$$

where  $I_{EQ}$  is the quiescent emitter current expressed in amperes.

First, the DPI seen looking into the base terminal of the transistor will be found. The DPI seen by the  $e_s$  signal source (Figure 6A) is  $R_B$  in series with the base DPI of transistor  $Q_1$ . Recognizing this fact permits us to move over to the base and drive it with an external generator, and then find the base DPI by solving for the current flowing from the external generator. This scheme is shown in the circuit of Figure 7 where base DPI =  $\frac{e_x}{i_x}$ .

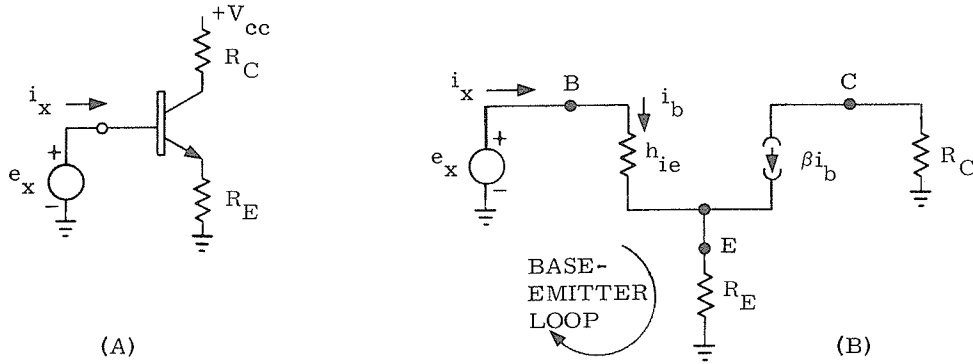


Figure 7. Base DPI of Bipolar Transistor

Using Kirchhoff's voltage law (KVL) around the base-emitter loop (Figure 7B), we have

$$i_b h_{ie} + i_b R_E + \beta i_b R_E - e_x = 0. \quad (32)$$

Observing  $i_b = i_x$  and solving for base DPI =  $\frac{e_x}{i_x}$  produces

$$\frac{e_x}{i_x} = \text{base DPI} = h_{ie} + (1 + \beta)R_E \quad (33)$$

Equation (33) can be interpreted as meaning that any impedance ( $R_E$ ) in the emitter lead of a bipolar transistor, when measured at the base terminal, will be increased by the factor  $(1 + \beta)$ .



The DPI seen looking into the emitter terminal of the bipolar transistor can be determined by driving the emitter with an external voltage source and solving for the generator current. The circuit is shown in Figure 8.

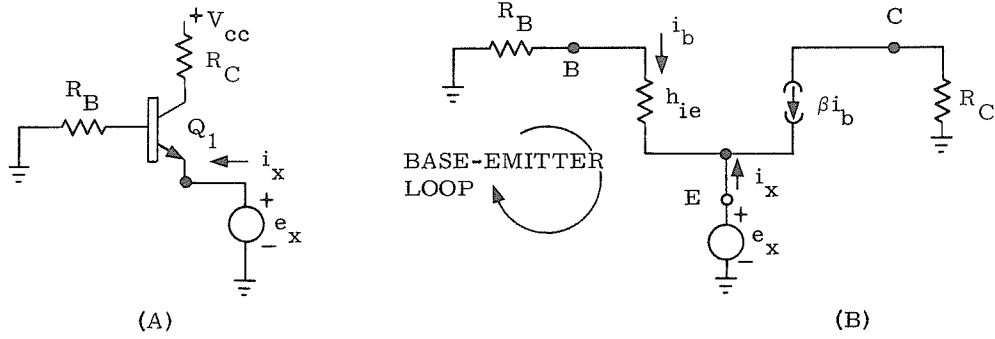


Figure 8. Emitter DPI of Bipolar Transistor

Using Kirchhoff's current law (KCL) at the emitter node and writing the KVL equation around the base-emitter loop will yield emitter DPI =  $\frac{e_x}{i_x}$ .

$$i_x + i_b + \beta i_b = 0.$$

$$i_x = -i_b(1 + \beta) \quad (34)$$

and

$$(h_{ie} + R_B)i_b + e_x = 0$$

$$i_b = -\frac{e_x}{h_{ie} + R_B} \quad (35)$$

So

$$\boxed{\frac{e_x}{i_x} = \text{emitter DPI} = \frac{h_{ie} + R_B}{(1+\beta)}} \quad (36)$$

Equation (36) indicates that any impedance ( $R_B$ ) connected to the base, as seen at the emitter, is diminished by the  $(1+\beta)$  factor.

The same procedure can be used to determine the collector DPI. From the simplified hybrid circuit model of the transistor (Figure 6B), it should be evident that the collector DPI is infinite since an external voltage source connected to the collector cannot excite a base current; therefore, the output from the  $\beta i_b$  generator will be zero.

$$\boxed{\text{collector DPI} = \infty} \quad (37)$$

Equations (33), (36), and (37) are fundamental to DPI analysis of bipolar transistor circuits. Summarizing, we have

$$\text{Base DPI} = h_{ie} + (1+\beta)R_E \quad (33)$$

$$\text{Emitter DPI} = \frac{h_{ie} + R_B}{(1+\beta)} \quad (36)$$

$$\text{Collector DPI} = \infty \quad (37)$$

The key to effectively applying these equations is to remember that the impedances  $R_B$  and  $R_E$  are the impedances seen by the base and emitter of the bipolar transistor respectively.  $R_B$  and  $R_E$  quite frequently are combinations of other circuit elements including transistors, FET's, etc. In addition to the DPI Equations, the basic relations between the base, emitter and collector currents of a bipolar transistor are indispensable to the analysis. These important relations are given below.

$$i_c = \beta i_b \quad (38)$$

$$i_e = (1+\beta)i_b \quad (39)$$

$$i_c = \left(\frac{\beta}{1+\beta}\right)i_e \quad (40)$$

Before DPI analysis is applied to an actual circuit, the DPI equation for a triode or pentode vacuum tube and J-FET will be derived. Note that these techniques are also applicable to the derivation of the DPI equations of other active devices.

#### Triode/Pentode Vacuum Tube DPI Equations

Figure 9 illustrates the circuit to be used for the determination of the vacuum tube DPI equations.

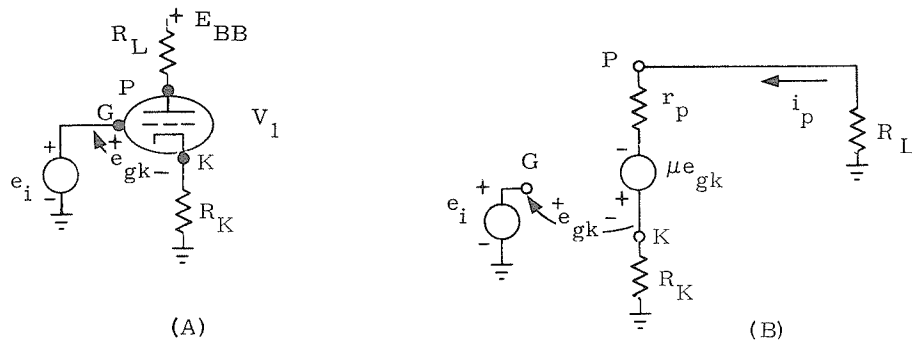


Figure 9. Circuit for the Determination of Vacuum Tube DPI Equations

$r_p$  is the dynamic plate resistance and  $\mu$  is the forward voltage amplification factor. Both of these parameters are defined at the quiescent operating point chosen for the tube.

$$r_p = \left. \frac{\partial v_{pk}}{\partial i_p} \right|_{v_{gk} = \text{Constant}} \quad (\text{ohms})$$

$$\mu = \left. \frac{-\partial v_{pk}}{\partial v_{gk}} \right|_{i_p = \text{Constant}} \quad (\text{dimensionless})$$

Inspection of the equivalent circuit of Figure 9(B) shows that the grid DPI is infinite (no grid current flows).

grid DPI =  $\infty$

(41)

Before the other equations are derived, an expression for the signal plate current will be found. This equation will be used frequently in the application of DPI analysis. Writing the KVL equation around the plate-cathode circuit (Figure 9B), we have

$$i_p r_p + i_p R_L + i_p R_K - \mu e_{gk} = 0 \quad . \quad (42)$$

but

$$e_{gk} = e_i - i_p R_K \quad . \quad (43)$$

Substituting Equation (43) into (42) gives

$$i_p r_p + i_p R_L + i_p R_K - \mu e_i + \mu i_p R_K = 0$$

$$i_p = \left( \frac{\mu e_i}{R_L + r_p + (1+\mu)R_K} \right)$$

(44)

To determine the plate DPI, we apply an external voltage source to the plate and find the current flow from this source as shown in Figure 10.

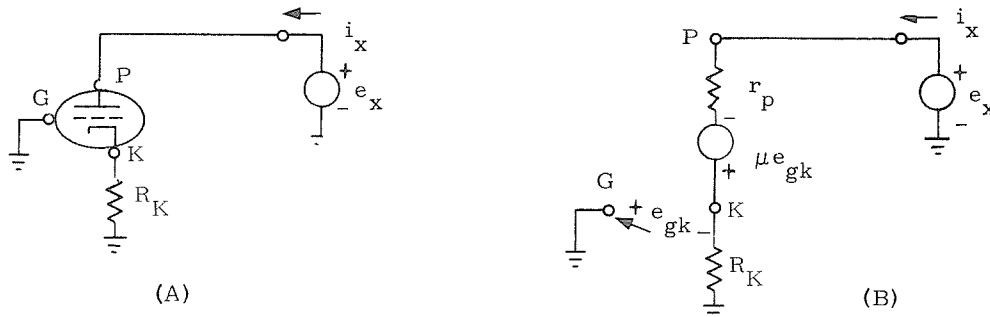


Figure 10. Determination of Plate DPI

Writing the KVL equation around the plate-cathode circuit, we have

$$i_x r_p - \mu e_{gk} + i_x R_K - e_x = 0 \quad . \quad (45)$$

But

$$e_{gk} = -i_x R_K \quad . \quad (46)$$

Substituting Equation (46) into (45) and solving for plate DPI =  $\frac{e_x}{i_x}$ , we have

$$i_x r_p - \mu(-i_x R_K) + i_x R_K = e_x \quad .$$

$$\boxed{\frac{e_x}{i_x} = \text{plate DPI} = r_p + (1+\mu)R_K} \quad (47)$$

Equation (47) indicates that any impedance ( $R_K$ ) connected to the cathode, as seen at the plate, is increased by the  $(1+\mu)$  factor.

The cathode DPI is found in a similar manner using the circuit of Figure 11.

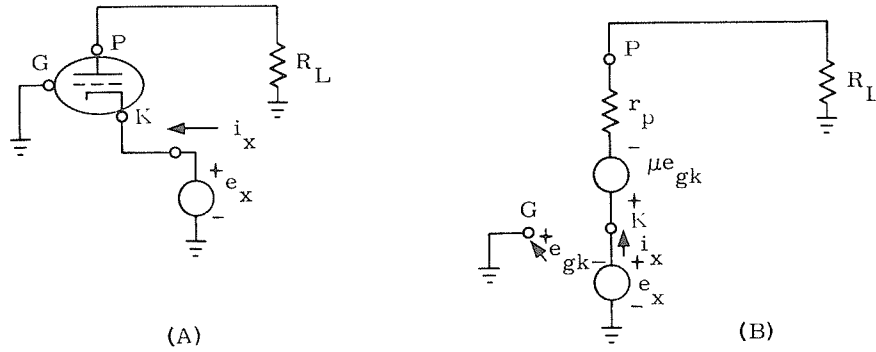


Figure 11. Determination of Cathode DPI

Writing the KVL equation around the plate-cathode circuit, we have

$$\mu e_{gk} + i_x r_p + i_x R_L - e_x = 0 \quad . \quad (48)$$

But

$$e_{gk} = -e_x \quad . \quad (49)$$

Substituting Equation (49) into (48) and solving for the cathode DPI =  $\frac{e_x}{i_x}$ , we have

$$-\mu e_x + i_x (r_p + R_L) - e_x = 0$$

$$\frac{e_x}{i_x} = \text{cathode DPI} = \left( \frac{r_p + R_L}{1 + \mu} \right) \quad (50)$$

Equation (50) indicates that any impedance ( $R_L$ ) connected to the plate, as seen at the cathode, is diminished by the  $(1+\mu)$  factor.

In summary, we have

$$i_p = \left( \frac{\mu e_i}{R_L + r_p + (1+\mu)R_K} \right) \quad (44)$$

$$\text{Grid DPI} = \infty \quad (41)$$

$$\text{Plate DPI} = (r_p + [1+\mu]R_K) \quad (47)$$

$$\text{Cathode DPI} = \left( \frac{r_p + R_L}{1 + \mu} \right) \quad (50)$$

Here, as in the case of the bipolar transistors, the important point to remember is that the  $R_L$  and  $R_K$  impedances can be other circuits containing active devices, i. e., transistors, vacuum tubes, etc.

#### J-FET DPI Equations

The circuit shown in Figure 12 will be used to derive the DPI equations for a J-FET (junction field-effect transistor). The operating region is defined such that no gate current flows.

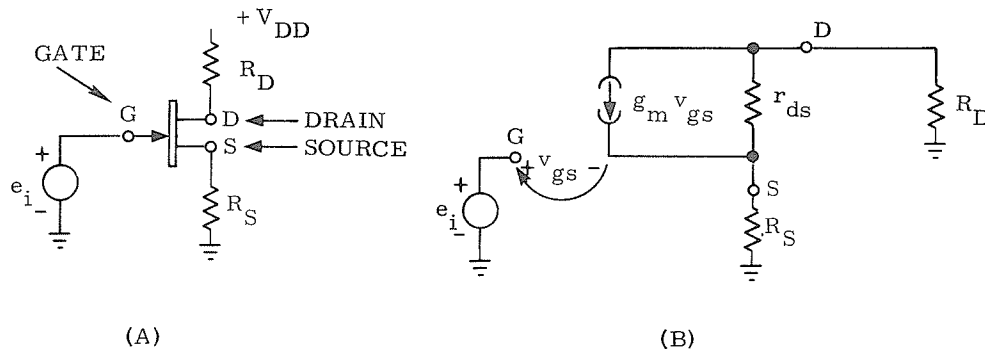


Figure 12. Circuit for Determination of J-FET DPI Equations

The FET equivalent circuit of Figure 12(B) can be made to assume the same form as the triode vacuum tube equivalent circuit of Figure 9(B) by the application of Thevenin's Theorem\* as shown in Figure 13.

\* Refer to Appendix A for a review of Thevenin's Theorem.

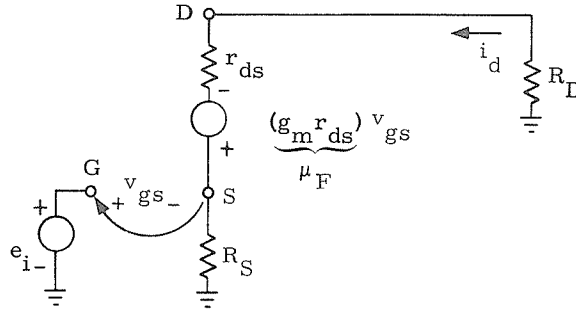


Figure 13. Thevenin Equivalent of FET Equivalent Circuit

Now if we define a voltage amplification factor  $\mu$  for the FET such that

$$\mu_F = g_m r_{ds} \quad (51)$$

then the DPI equations for the FET take on exactly the same form as the triode vacuum tube equations and the same remarks apply. The FET DPI equations follow:

$$i_d = \left( \frac{\mu_F e_i}{R_D + r_{ds} + (1 + \mu_F) R_S} \right) \quad (52)$$

$$\text{Gate DPI} = \infty \quad (53)$$

$$\text{Source DPI} = \frac{r_{ds} + R_D}{(1 + \mu_F)} \quad (54)$$

$$\text{Drain DPI} = r_{ds} + (1 + \mu_F) R_S \quad (55)$$

$r_{ds}$  is the dynamic drain-to-source resistance and corresponds to  $r_p$  of the vacuum tube.  $\mu_F$  is the voltage amplification factor, and  $g_m$  is the transconductance of the FET. These parameters are defined in the same manner as they are for the triode vacuum tube, i.e.,

$$r_{ds} = \left. \frac{\partial v_{ds}}{\partial i_d} \right|_{v_{gs} = \text{Constant}} \quad (\text{ohms}) \quad (56)$$

$$\mu_F = \left. \frac{-\partial v_{ds}}{\partial v_{gs}} \right|_{i_d = \text{Constant}} \quad (\text{dimensionless}) \quad (57)$$

$$g_m = \left. \frac{\partial i_d}{\partial v_{gs}} \right|_{v_{ds} = \text{Constant}} \quad (\text{mhos}) \quad (58)$$

These parameters are all defined at the quiescent operating point.

In most cases,  $r_{ds}$  can be assumed to be infinite. This greatly simplifies the DPI equations for the FET. The effect of letting  $r_{ds}$  go to infinity can be seen by substituting the expression for  $\mu_F$  (Equation 51) into Equations (52), (54), and (55) and taking the limit as  $r_{ds}$  goes to infinity.

$$\lim_{r_{ds} \rightarrow \infty} i_d = \lim_{r_{ds} \rightarrow \infty} \left( \frac{g_m r_{ds} e_i}{R_D + r_{ds} + (1 + g_m r_{ds}) R_S} \right) = \left( \frac{e_i}{\frac{R_D}{g_m r_{ds}} + \frac{1}{g_m} + \frac{R_S}{g_m r_{ds}} + R_S} \right)$$

$$= \left( \frac{e_i}{\frac{1}{g_m} + R_S} \right)$$

$$\boxed{i_d = \frac{e_i}{\frac{1}{g_m} + R_S}} \quad \begin{array}{l} (52-A) \\ \text{IDEAL FET} \end{array}$$

$$\lim_{r_{ds} \rightarrow \infty} \text{DPI}_{\text{Source}} = \lim_{r_{ds} \rightarrow \infty} \left( \frac{r_{ds} + R_D}{1 + g_m r_{ds}} \right) = \lim_{r_{ds} \rightarrow \infty} \left( \frac{1 + \frac{R_D}{r_{ds}}}{\frac{1}{r_{ds}} + g_m} \right)$$

$$= \frac{1}{g_m}$$

$$\boxed{\text{Source DPI} = \frac{1}{g_m}} \quad \begin{array}{l} (54-A) \\ \text{IDEAL FET} \end{array}$$

$$\lim_{r_{ds} \rightarrow \infty} \text{DPI}_{\text{Drain}} = \lim_{r_{ds} \rightarrow \infty} \left( r_{ds} + (1 + g_m r_{ds}) R_S \right) = \infty$$

$$\boxed{\text{Drain DPI} = \infty} \quad \begin{array}{l} (55-A) \\ \text{IDEAL FET} \end{array}$$

A summary of the ideal FET equations follows:

$i_d = \frac{e_i}{\frac{1}{g_m} + R_S}$	(52-A)	IDEAL FET DPI EQUATIONS
$\text{Gate DPI} = \infty$	(53)	
$\text{Source DPI} = \frac{1}{g_m}$	(54-A)	
$\text{Drain DPI} = \infty$	(55-A)	

In the examples that follow, both sets of equations will be used but it should be emphasized that in most cases, the ideal FET equations are sufficient for most engineering calculations.

## Application of DPI Analysis to Some Simple Transistor Circuits

### Series Parallel Networks

All of the basic tools needed to effectively apply DPI analysis to a wide variety of electronic circuits have been covered. A sampling of how DPI analysis can be utilized on a variety of circuits will now be presented. Feedback circuits will be covered later. The first circuit to be analyzed is shown in Figure 14.

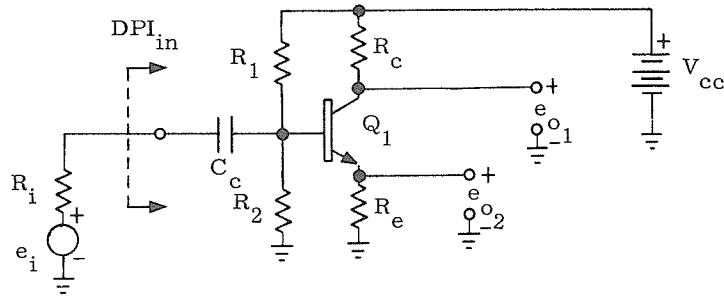


Figure 14. Single Stage Transistor Amplifier

Assume that the DPI looking in at the input and both output ports, and also the voltage gains, are required. The input DPI is the capacitive reactance of  $C_c$  in series with the parallel combination of  $R_1$ ,  $R_2$  and the base DPI of  $Q_1$ . The complete expression for the  $DPI_{in}$  seen by the signal source is given in Equation (59), which was written in a single step by inspection.

$$DPI_{in} = \left( \frac{1}{j\omega C_c} \right) + \left\{ (R_1 \parallel R_2) \parallel \underbrace{\left( h_{ie} + [1+\beta] R_e \right)}_{\text{Base DPI}} \right\} \quad (59)$$

The DPI at the  $e_{o1}$  terminal is  $R_c$  since the collector DPI =  $\infty$ .

$$DPI_{e_{o1}} = R_c \quad (60)$$

The DPI at the  $e_{o2}$  terminal is  $R_e$  in parallel with the emitter DPI.

$$DPI_{e_{o2}} = (R_e) \parallel \left\{ \underbrace{\frac{h_{ie} + (R_1 \parallel R_2) \parallel \left( \frac{1}{j\omega C_c} + R_i \right)}{(1+\beta)}}_{\text{Emitter DPI}} \right\} \quad (61)$$



If only mid-band frequencies are considered, the capacitive reactance terms in Equations (59) and (61) can be dropped. The mid-band signal voltage gains  $\frac{e_{o1}}{e_i}$  and  $\frac{e_{o2}}{e_i}$  will be written by inspection.

$+V_{cc}$  is always assumed to be at signal ground.

$$e_{o1} = - \left[ \underbrace{\frac{e_i}{R_i + \left\{ (R_1 \parallel R_2) \parallel (h_{ie} + [1+\beta] R_e) \right\}}}_{\text{Current } i_i \text{ flowing from signal source } e_i} \right] \left[ \underbrace{\frac{(R_1 \parallel R_2)}{(R_1 \parallel R_2) + (h_{ie} + [1+\beta] R_e)}}_{\text{Current divider to find portion of } i_i \text{ flowing to base of } Q_1} \right] \beta R_c \quad (62)$$

$i_b$   
 Base current of  $Q_1$

$i_c$   
 Collector current of  $Q_1$

$$e_{o1} = -i_c R_c$$

Signal output voltage at terminal  $e_{o1}$

$$e_{o2} = \left[ \underbrace{\frac{e_i}{R_i + \left\{ (R_1 \parallel R_2) \parallel (h_{ie} + [1+\beta] R_e) \right\}}}_{\text{Current } i_i \text{ flowing from signal source } e_i} \right] \left[ \underbrace{\frac{(R_1 \parallel R_2)}{(R_1 \parallel R_2) + (h_{ie} + [1+\beta] R_e)}}_{\text{Current divider to find portion of } i_i \text{ flowing to base of } Q_1} \right] (1+\beta) R_e \quad (63)$$

$i_b$   
 Base current of  $Q_1$

$i_e$   
 Emitter current of  $Q_1$

$$e_{o2} = i_e R_e$$

Signal output voltage at terminal  $e_{o2}$

Equations (62) and (63) are derived as follows. The signal output voltage is determined by the current flowing through the load impedance ( $R_c$  or  $R_e$  for  $e_{o1}$  or  $e_{o2}$ ). Both the emitter and collector signal currents depend upon the signal base current, but the signal base current is determined by the total current flowing from the signal source  $e_i$ ; therefore, to find either the emitter or collector signal current, the first step is to find the total signal current  $i_i$  that flows from the  $e_i$  signal source. Once  $i_i$  is known, a current divider fraction can be written to determine what portion of  $i_i$  flows into the base of  $Q_1$ . With the base current known, the collector or emitter current can be found by multiplying by  $\beta$  or  $(1+\beta)$  respectively. The last step is, of course, to multiply by the respective load impedance,  $R_c$  or  $R_e$ . The correct phase must be determined by tracing the currents through the circuit, e.g., a current into the base of  $Q_1$  causes a current into the collector of  $Q_1$ , which causes  $e_{o1}$  to decrease with respect to ground; thus, there is a  $180^\circ$  phase reversal as noted in Equation (62). It should be obvious at this point that it is far more tedious to explain DPI analysis than it is to apply it.

The dc quiescent conditions existing in the circuit of Figure 14 can also be determined with DPI analysis. The dc analysis of bipolar transistor circuits requires that the base-emitter dc offset voltage be taken into consideration. If silicon transistors are being used, the offset voltage is in the range of 0.6 to 0.7 volt. The dc circuit of the single stage amplifier (Figure 14) is shown in Figure 15 with the  $R_1$ ,  $R_2$  bias network replaced by its Thevenin's equivalent circuit.

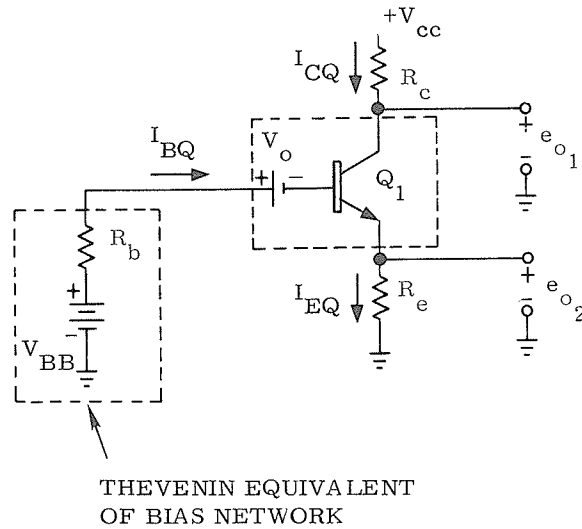


Figure 15. DC Circuit of Single-Stage Amplifier

Note that the dc offset voltage of the base-emitter junction is treated as if it were a battery connected in series with the base terminal.

To find the quiescent base current  $I_{BQ}$ , we write the KVL equation around the base-emitter loop using the fact that we know the base DPI of  $Q_1$ .

$$I_{BQ} \left( R_b + h_{ie} + (1+\beta)R_e \right) + V_o - V_{BB} = 0$$

$$I_{BQ} = \left( \frac{V_{BB} - V_o}{R_b + h_{ie} + (1+\beta)R_e} \right) \quad (64)$$

Recalling that  $I_{CQ} = \beta I_{BQ}$  and  $I_{EQ} = (1+\beta)I_{BQ}$ , we have expressions for all of the quiescent currents; knowing these currents permits us to write the expressions for the quiescent output voltages as shown in Equations (65) and (66).

$$E_{o1Q} = V_{CC} - I_{CQ}R_c \quad (65)$$

$$E_{o2Q} = I_{EQ}R_e \quad (66)$$

At this point, a note about biasing the circuit of Figure 14 is in order. Good design practice demands that the values of  $E_{o1Q}$  and  $E_{o2Q}$  (quiescent values of output voltage) remain relatively constant for a wide range of  $\beta$ 's. In other words, the value of quiescent collector current should be as independent of  $\beta$  as is possible to permit changing the transistor without having to alter the circuit components. It seems to be common practice to use "rules of thumb" for biasing circuits. Unfortunately, it is also quite common to find designers applying these rules to circuits or under conditions where the original assumptions do not apply. Circuit equations are so simple to derive utilizing DPI analysis that it is easier to write and analyze the equations of interest than it is to remember "handy-dandy" formulas.

As an example, let us consider what conditions must be met in order to maintain a constant  $I_{CQ}$  in the circuit of Figure 15. By multiplying the expression for the quiescent base current (Equation 64) by  $\beta$ , we have an expression for  $I_{CQ}$ .

$$I_{CQ} = \beta I_{BQ} = \beta \left( \frac{V_{BB} - V_o}{R_b + h_{ie} + (1+\beta)R_e} \right) \quad (67)$$

Manipulating Equation (67) yields

$$I_{CQ} = \frac{\left( \frac{V_{BB} - V_o}{\beta} \right)}{\left[ \frac{R_b + h_{ie}}{\beta} + \left[ \frac{(1+\beta)}{\beta} R_e \right] \right]} \quad (68)$$

Now, we must examine Equation (68) in order to see how we can force it to be independent of  $\beta$ . Examining the denominator, we see that two terms are a function of  $\beta$ . It is usually a good approximation to assume that  $\frac{(1+\beta)}{\beta} \approx 1$  for high  $\beta$  transistors, i.e., if  $\beta = 40$ , then  $41/40 = 1.025 \approx 1.0$ . If we make this assumption, the denominator term containing  $R_e$  is

relatively independent of  $\beta$ . It is also easy to see that if  $R_e$  is made much much greater than  $\frac{R_b + h_{ie}}{\beta}$ , Equation (68) will be relatively independent of  $\beta$ . Furthermore, it is usually valid to assume that  $h_{ie}/\beta$  is small enough compared to  $R_b/\beta$  that the former can be left out of the expression. We then have  $R_e \gg \frac{R_b}{\beta}$  or  $\beta R_e \gg R_b$  for good stability of  $I_{CQ}$ .

As a further example, consider the circuit shown in Figure 16 and determine the mid-band voltage gain by writing the solution in a single step. At mid-band frequencies the coupling and by-pass capacitors can be considered to be signal short circuits. The voltage gain expression is given in Equation (69).

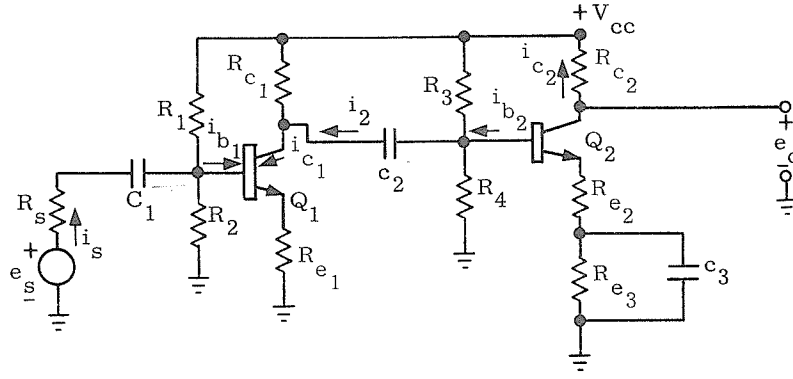


Figure 16. Two-Stage RC Coupled Amplifier

$$e_o = \left[ \frac{e_s}{R_s + \underbrace{\{(R_1 \parallel R_2) \parallel (h_{ie1} + [1 + \beta_1] R_{e1})\}}_{\text{Base 1 DPI}}} \right] \underbrace{\left[ \frac{(R_1 \parallel R_2)}{(R_1 \parallel R_2) + (h_{ie1} + [1 + \beta_1] R_{e1})} \right]}_{\text{Current divider fraction}} \beta_1 \underbrace{\left[ \frac{R_{c1}}{R_{c1} + \underbrace{\{(R_3 \parallel R_4) \parallel (h_{ie2} + [1 + \beta_2] R_{e2})\}}_{\text{Base 2 DPI}}} \right]}_{\text{Current divider fraction}} \underbrace{\left[ \frac{R_3 \parallel R_4}{(R_3 \parallel R_4) + (h_{ie2} + [1 + \beta_2] R_{e2})} \right]}_{\text{Current divider fraction}} \beta_2 R_{c2} \quad (69)$$

$i_s$  Signal source current  
 $i_{b1}$  Signal base current  
 $i_{c1}$  Signal collector current  
 $i_2$  Portion of signal collector current flowing toward  $Q_2$  base  
 $i_{b2}$  Signal base current  
 $i_{c2}$  Signal collector current

Equation (69) is developed as follows. The signal output voltage  $e_o$  is produced by  $i_{c2}$  flowing through  $R_{c2}$ , but  $i_{c2}$  is determined by  $i_{b2}$ . The signal base current  $i_{b2}$  is a fraction of  $i_{c1}$ ,

but  $i_{c1}$  is determined by  $i_{b1}$ , which, in turn, is a fraction of the signal source current  $i_s$ .  $i_s$  is, of course, determined by  $e_s$ , the signal source. When writing the expression for  $e_o$  as a function of  $e_s$ , the first step is to determine the signal source current  $i_s$ . With  $i_s$  known,  $i_{b1}$  can be found by multiplying  $i_s$  by a current divider fraction to determine the portion of  $i_s$  which flows to the base of  $Q_1$ .  $i_{c1}$  is  $\beta i_{b1}$ , and  $i_2$  can be found by multiplying by another current divider fraction. An additional current divider fraction produces the  $i_{b2}$  signal base current, and  $i_{c2}$  is given by the  $\beta i_{b2}$  product. Finally,  $e_o$  is found by multiplying by  $R_{c2}$ .

A basic building block of many integrated and discrete circuits is the emitter-coupled differential amplifier shown in Figure 17.

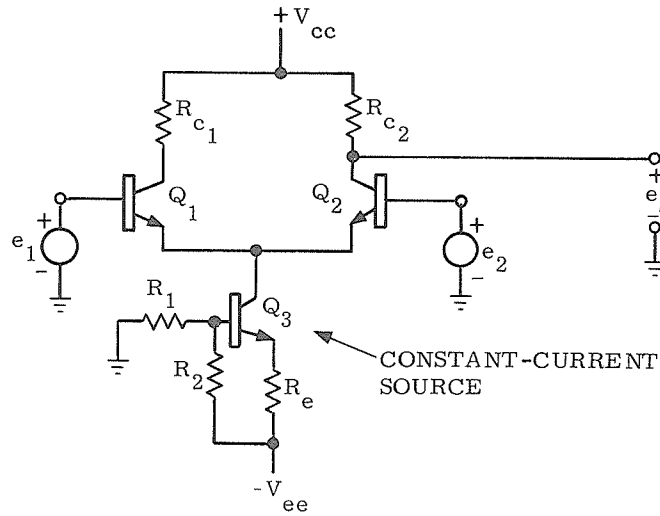


Figure 17. Basic Emitter-Coupled Differential Amplifier

Using DPI analysis and the superposition theorem, the output voltage as a function of the two input voltages can be written by inspection. The result is shown in Equation (70).

$$e_o = \underbrace{\left[ \frac{e_1}{h_{ie1} + (1+\beta_1) \left[ \frac{h_{ie2}}{1+\beta_2} \right]} \right]}_{\substack{\text{Signal base current } i_{b1} \\ \text{Signal emitter } Q_1 \text{ current} \\ \text{due to } e_1 \text{ acting alone}}} \underbrace{\left( (1+\beta_1) \left( \frac{\beta_2}{1+\beta_2} \right) R_{c2} \right)}_{\substack{\text{Signal } Q_2 \text{ collector current} \\ \text{due to source } e_1 \text{ acting alone}}} + \underbrace{\left[ \frac{e_2}{h_{ie2} + (1+\beta_2) \left[ \frac{h_{ie1}}{1+\beta_1} \right]} \right]}_{\substack{\text{Signal base current } i_{b2} \\ \text{Signal collector } Q_2 \\ \text{current due to } e_2 \\ \text{acting alone}}} \underbrace{\left( \beta_2 R_{c2} \right)}_{\substack{\text{Portion of } e_o \text{ due to signal } e_2 \\ \text{acting alone}}} \quad (70)$$

Portion of  $e_o$  due to signal  $e_1$  acting alone

To obtain Equation (70) we utilize the superposition theorem. We replace voltage signal source  $e_2$  by its internal impedance (short circuit) and solve for the portion of  $e_o$  which is caused by signal source  $e_1$ ; then, voltage signal source  $e_1$  is replaced by its internal impedance (short circuit), and the portion of  $e_o$  which is caused by signal source  $e_2$  is found. The sum of these two terms gives the output voltage  $e_o$  as a function of the two input signals  $e_1$  and  $e_2$  and the circuit parameters. Setting  $e_2 = 0$  we find the current flowing from the  $e_1$  signal source which is the signal base current of  $Q_1$ . The signal emitter current of  $Q_1$  is found by multiplying  $i_{b1}$  by  $(1 + \beta_1)$ . All of the signal emitter current of  $Q_1$  flows into the  $Q_2$  emitter since the DPI of collector  $Q_3$  is infinite. Collector  $Q_2$  signal current is  $(\beta_2 / (1 + \beta_2))$  times the  $Q_2$  signal emitter current. Multiplying the whole expression by collector load  $R_{c2}$  yields the portion of  $e_o$  due to  $e_1$ . Setting  $e_1 = 0$  we find the current flowing from the  $e_2$  signal source which is the signal base current of  $Q_2$ . Multiplying the signal base current of  $Q_2$  by  $\beta_2$  produces the signal collector current of  $Q_2$ , and multiplying by  $R_{c2}$  produces the portion of  $e_o$  due to  $e_2$ . Checking current directions will show that  $e_1$  is connected to the noninverting side of the amplifier while  $e_2$  is connected to the inverting side.

The circuit of Figure 18 is an FET source-coupled differential amplifier using FET's in place of the transistors  $Q_1$  and  $Q_2$  of Figure 17. The voltage gain of this amplifier is given in Equation (71) without further explanation. The reasoning process is very similar to that used for deriving the gain of the circuit of Figure 17.

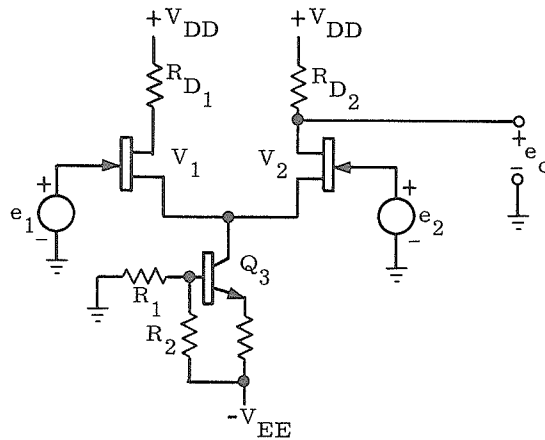


Figure 18. Basic Source-Coupled Differential Amplifier

$$e_o = \left\{ \frac{\mu_{F_1} e_1}{r_{ds_1} + R_{D_1} + (1 + \mu_{F_1}) \left[ \frac{r_{ds_2} + R_{D_2}}{(1 + \mu_{F_2})} \right]} \right\} R_{D_2} - \left\{ \frac{\mu_{F_2} e_2}{r_{ds_2} + R_{D_2} + (1 + \mu_{F_2}) \left[ \frac{r_{ds_1} + R_{D_1}}{(1 + \mu_{F_1})} \right]} \right\} R_{D_2} \quad (71)$$

If the ideal FET equations are applied to the solution of this circuit, the expression for  $e_o$  is given in Equation (71-A). It can be seen that utilization of the ideal FET DPI equations greatly simplifies the form of the resulting circuit solutions.

$$e_o = \left\{ \frac{e_1}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \right\} R_{D_2} - \left\{ \frac{e_2}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}} \right\} R_{D_2} \quad (71-A)$$

$$= (e_1 - e_2) \left\{ \frac{R_{D_2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \right\} \quad (71-B)$$

The form of Equation (71-B) clearly demonstrates why this amplifier is called a difference amplifier.

### Nonseries Parallel Networks

Thus far, only simple series parallel type networks have been used as examples. Quite frequently, networks are encountered which can not be so easily classified. Consider the circuit shown in Figure 19 and observe that neither the voltage divider nor the current divider equation will permit the answer to be written directly by inspection. Of course, conventional node or loop analysis techniques will yield the desired answer, but our object is to avoid this approach because the form of the resultant equations is not as clear and easily interpreted as are voltage or current divider equations.  $\Delta$  - Y transformations will also be avoided because they are not readily performed in a single step, and rarely are they remembered. The object here will be to familiarize the reader with a technique which can be applied to the solution of circuits containing feedback.

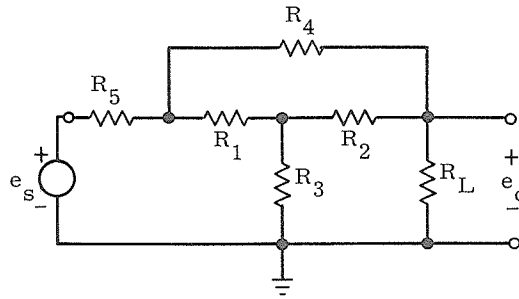


Figure 19. Simple Nonseries Parallel Circuit

The circuit of Figure 20 is the same as the one shown in Figure 19 except for the addition of the  $e_x$  voltage generator to the  $e_o$  terminal.

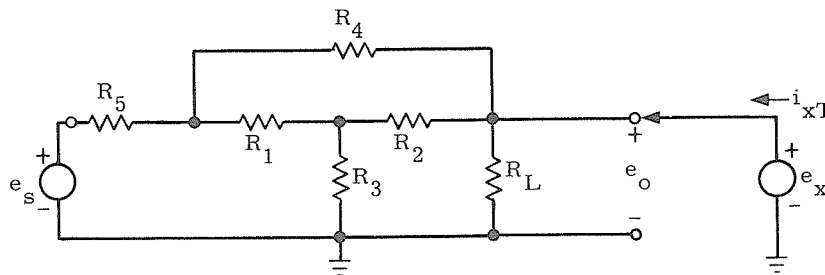


Figure 20. Simple Nonseries Parallel Circuit

An expression for  $e_o$  can be easily found by using superposition. Solve for the current  $i_{xT}$  by using the superposition theorem;  $i_{xT}$  will be composed of two parts:

$$i_{xT} = (e_s, e_x = 0) + i_x(e_s = 0, e_x) \quad (72)$$

The first part of  $i_{xT}$  is due to  $e_s$  when  $e_x = 0$ , and the second part is due to  $e_x$  when  $e_s = 0$ .



Several things should be noted about Equation (72). When  $e_s = 0$ ,  $i_x$  due to  $e_x$  has the form

$$i_x(e_x) = \frac{e_x}{(\text{factor})}$$

Dimensional analysis will reveal that the (factor) must be an impedance, and, in fact, the (factor) turns out to be the output driving-point-impedance seen looking into the output terminals. When  $e_x = 0$ ,  $i_x$  due to  $e_s$  is the output short circuit current. Equation (72) can now be rewritten as

$$i_{xT} = i_{osc} + \frac{e_x}{R_o} \quad (73)$$

where  $i_{osc}$  is the output short circuit current, and  $R_o$  is the output driving-point-impedance. Because  $e_x$  is a fictitious external generator, it can be adjusted to assume any convenient value. If  $e_x$  is adjusted so that it assumes the value of  $e_o$ , this forces the current flowing from the  $e_x$  generator to be zero. If this is not obvious, consider the circuit of Figure 21.

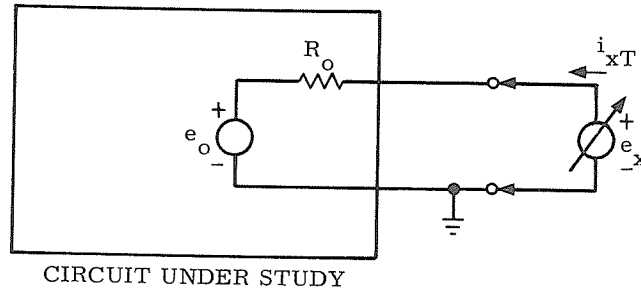


Figure 21.

As soon as the  $e_x$  generator is adjusted so that  $e_x = e_o$ ,  $i_{xT}$  will be forced to zero and removing  $e_x$  will have no effect. Applying the superposition theorem to the circuit of Figure 21 and solving for  $i_{xT}$ , we have

$$i_{xT} = \frac{e_x}{R_o} - \frac{e_o}{R_o} \quad (74)$$

Setting  $e_x = e_o$  forces  $i_{xT} = 0$ .

Assume now that we have set  $e_x = e_o$  such that  $i_{xT} = 0$ . This forces Equation (73) to become

$$0 = i_{osc} + \frac{e_o}{DPI_{out}} \quad (75)$$

Now Equation (75) can be solved for  $e_o$ ,

$$e_o = -i_{osc} DPI_{out} \quad (76)$$

where the  $R_o$  term has been replaced by the more descriptive  $DPI_{out}$  term. The method used to derive Equation (76) should be thoroughly understood because it is the basis for handling feedback circuits using DPI analysis. This method will now be used to solve the circuit of Figure 20, which is repeated in Figure 22. The answer will be developed in steps to demonstrate the technique.

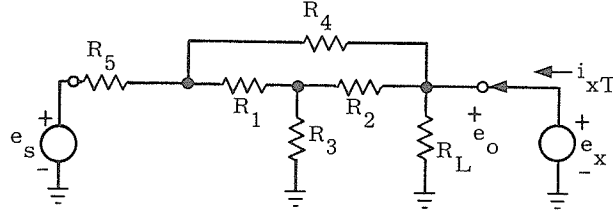


Figure 22. Simple Nonseries Parallel Circuit

$i_{xT} = i_{osc} + \frac{e_x}{DPI_o}$  by the superposition theorem. Solving for  $i_{osc}$  shown in Figure 23, we have Equation (77).

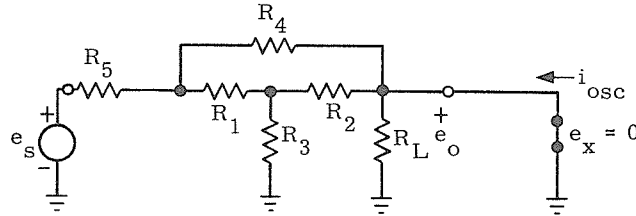


Figure 23. Solving for Current  $i_{osc}$

$$i_{osc} = \underbrace{\left\{ \frac{e_s}{R_5 + [R_4 \parallel \{R_1 + (R_2 \parallel R_3)\}]} \right\}}_{\text{Total current } i_s \text{ from } e_s} \underbrace{\left\{ - \left( \frac{R_1 + [R_2 \parallel R_3]}{[R_1 + [R_2 \parallel R_3]] + R_4} \right) \right\}}_{\text{Portion of } i_s \text{ flowing through } R_4 \text{ and contributing to } i_{osc}} \underbrace{\left\{ - \left( \frac{R_4}{R_4 + (R_1 + [R_2 \parallel R_3])} \right) \left( \frac{R_3}{R_2 + R_3} \right) \right\}}_{\text{Portion of } i_s \text{ flowing through } R_2 \text{ and contributing to } i_{osc}} \quad (77)$$

Now we solve for the other part of  $i_{xT}$ , which is  $e_x/DPI_{out}$ , by replacing  $e_s$  by its internal impedance as shown in Figure 24.

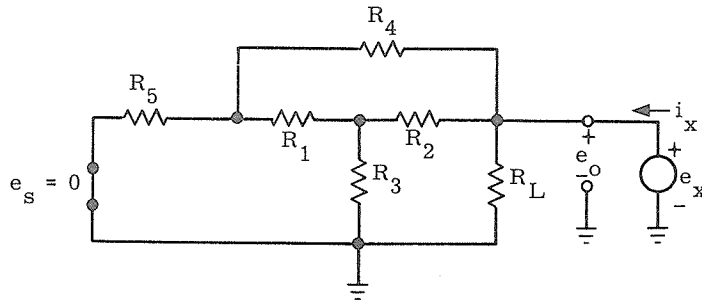


Figure 24. Solving for Current  $i_x(e_x)$

In order to obtain the solution for the  $i_x$  current, we apply an external generator to each circuit element connected to the  $e_o$  node as shown in Figure 25.

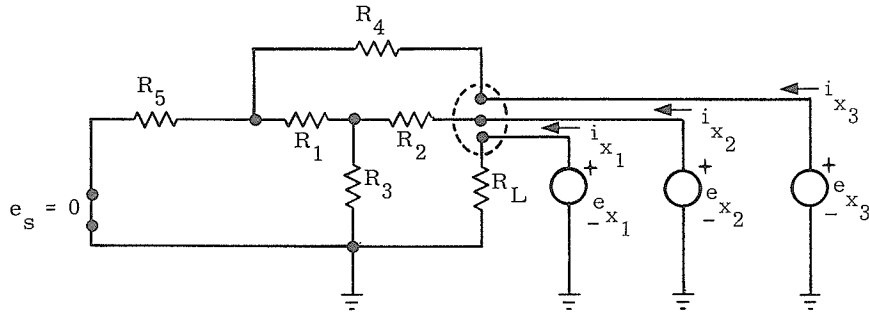


Figure 25. Solving for  $i_x(e_x)$  by Using Multiple External Sources

Once expressions for  $i_{x1}$ ,  $i_{x2}$ , and  $i_{x3}$  have been found by using the superposition theorem,  $e_{x1}$ ,  $e_{x2}$  and  $e_{x3}$  can be set equal to  $e_x$ , and then the sum of  $i_{x1}$ ,  $i_{x2}$ , and  $i_{x3}$  will yield  $i_x(e_x)$ . Using functional notation, the expression for  $i_x(e_x)$  is given by Equation (78).

$$\begin{aligned}
 i_x = & \underbrace{i_{x1}(e_{x1}) + i_{x2}(e_{x1}) + i_{x3}(e_{x1})}_{\substack{\text{Currents caused by } e_{x1} \\ \text{source} = i_{x1}}} + \underbrace{i_{x1}(e_{x2}) + i_{x2}(e_{x2}) + i_{x3}(e_{x2})}_{\substack{\text{Currents caused by } e_{x2} \\ \text{source} = i_{x2}}} + \underbrace{i_{x1}(e_{x3}) + i_{x2}(e_{x3}) + i_{x3}(e_{x3})}_{\substack{\text{Currents caused by } e_{x3} \\ \text{source} = i_{x3}}} \quad (78)
 \end{aligned}$$

Inspection of Figure 25 will show that many of the terms of Equation (78) are equal to zero, namely,  $i_{x2}(e_{x1})$ ,  $i_{x3}(e_{x1})$ ,  $i_{x1}(e_{x2})$  and  $i_{x1}(e_{x3})$ .

Solving for  $i_{x_1}$ ,  $i_{x_2}$ , and  $i_{x_3}$  by superposition to find  $i_x$ , we have

$$i_x = \frac{e_{x_1}}{R_L} + 0 + 0 + 0 + \left( \frac{e_{x_2}}{R_2 + \left\{ R_3 \parallel (R_1 + [R_4 \parallel R_5]) \right\}} \right) \left( 1 - \left\{ \frac{R_3}{R_3 + [R_1 + (R_4 \parallel R_5)]} \right\} \left\{ \frac{R_5}{R_4 + R_5} \right\} \right) + 0 + \left( \frac{e_{x_3}}{R_4 + \left\{ R_5 \parallel (R_1 + (R_2 \parallel R_3)) \right\}} \right) \left( 1 - \left\{ \frac{R_5}{R_5 + [R_1 + (R_2 \parallel R_3)]} \right\} \left\{ \frac{R_3}{R_3 + R_2} \right\} \right) \quad (79)$$

Now, setting  $e_{x_1} = e_{x_2} = e_{x_3} = e_x$  and getting Equation (79) in the form  $i_x(e_x) = \frac{e_x}{DPI_o}$ , we have the portion of  $i_{xT}$  (Figure 24) caused by the  $e_x$  source.

$$i_x = e_x \left\{ \frac{1}{R_L} + \frac{1}{\left\{ \frac{R_2 + \left\{ R_3 \parallel (R_1 + [R_4 \parallel R_5]) \right\}}{1 - \left\{ \frac{R_3}{R_3 + [R_1 + (R_4 \parallel R_5)]} \right\} \left\{ \frac{R_5}{R_4 + R_5} \right\}} \right\}} + \frac{1}{\left\{ \frac{R_4 + \left\{ R_5 \parallel (R_1 + (R_2 \parallel R_3)) \right\}}{1 - \left\{ \frac{R_5}{R_5 + [R_1 + (R_2 \parallel R_3)]} \right\} \left\{ \frac{R_3}{R_3 + R_2} \right\}} \right\}} \right\} \quad (80)$$

The expression for the output DPI can be taken from Equation (80) by observing that the terms within the large braces must each have the dimensions of 1/ohms. Recalling that the total impedance of many parallel impedances is given by Equation (81), we can see that the  $DPI_{out}$  from Equation (80) is given in Equation (82).

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} = \frac{1}{R_1 \parallel R_2 \parallel R_3} \quad (81)$$

$$DPI_{out} = R_L \parallel \left\{ \frac{R_2 + \left\{ R_3 \parallel (R_1 + [R_4 \parallel R_5]) \right\}}{1 - \left\{ \frac{R_3}{R_3 + [R_1 + (R_4 \parallel R_5)]} \right\} \left\{ \frac{R_5}{R_5 + R_4} \right\}} \right\} \parallel \left\{ \frac{R_4 + \left\{ R_5 \parallel (R_1 + (R_2 \parallel R_3)) \right\}}{1 - \left\{ \frac{R_5}{R_5 + [R_1 + (R_2 \parallel R_3)]} \right\} \left\{ \frac{R_3}{R_3 + R_2} \right\}} \right\} \quad (82)$$

Using Equation (76), and substituting into it the expressions for  $DPI_{out}$  and  $-i_{osc}$  from Equations (77) and (82), we have the complete expression for  $e_o$  as a function of  $e_s$  as shown in Equation (83).

$$e_o = \underbrace{\left( \left\{ \frac{e_s}{R_5 + [R_4 \parallel \{R_1 + (R_2 \parallel R_3)\}]} \right\} \left\{ \frac{R_1 + [R_2 \parallel R_3]}{R_1 + [R_2 \parallel R_3] + R_4} + \left( \frac{R_4}{R_4 + R_1 + [R_2 \parallel R_3]} \right) \left( \frac{R_3}{R_3 + R_2} \right) \right\} \right)}_{-i_{osc}} \underbrace{\left\{ R_L \parallel \left\{ \frac{R_2 + \{R_3 \parallel \{R_1 + [R_4 \parallel R_5]\}\}}{1 - \left\{ \frac{R_3}{R_3 + [R_1 + (R_4 \parallel R_5)]} \right\} \left\{ \frac{R_5}{R_5 + R_4} \right\}} \right\} \parallel \left\{ \frac{R_4 + (R_5 \parallel \{R_1 + (R_2 \parallel R_3)\})}{1 - \left\{ \frac{R_5}{R_5 + [R_1 + (R_2 \parallel R_3)]} \right\} \left\{ \frac{R_3}{R_3 + R_2} \right\}} \right\} \right\}}_{DPI_O} \quad (83)$$

At this point it is probably not at all evident that the use of DPI analysis to obtain Equation (83) has any advantage over loop or node analysis. In reality, it would be ridiculous to solve this circuit (Figure 19) by DPI analysis; the actual value of this approach will not be evident until feedback circuits are investigated.

### Application of DPI Analysis to a Feedback Amplifier

The feedback amplifier of Figure 26 will be analyzed using DPI analysis and the technique presented for handling nonseries parallel circuits.

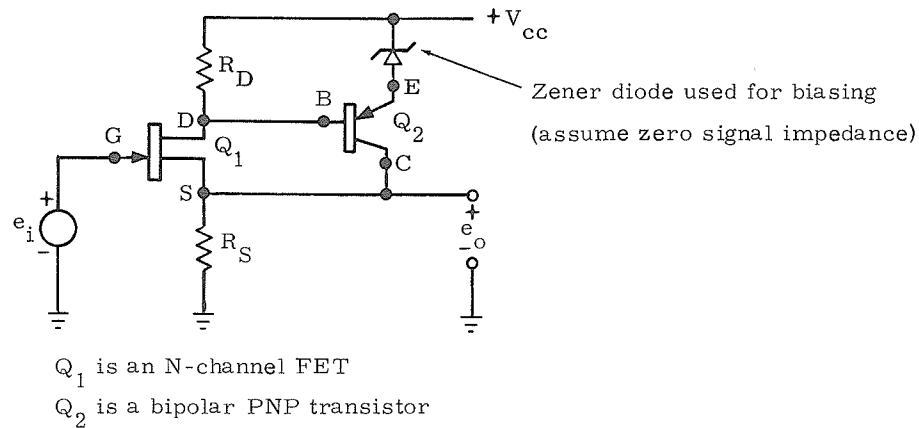


Figure 26. Amplifier Circuit Containing Feedback

The circuit of Figure 26 is classified as a feedback circuit because a portion of the output current is fed back to the input in such a way as to modify the conditions existing in the input circuitry. In this case, the collector current of Q<sub>2</sub> modifies the source current of Q<sub>1</sub>. Assume for the moment that the output impedance of this amplifier is needed. The inexperienced user of DPI analysis would look into the output terminal and say that the output DPI is just R<sub>s</sub> in parallel

with the source DPI of the FET  $Q_1$ . This answer will be shown to be incorrect because the feedback causes the output impedance to be modified. The DPI equations needed for the analysis of this circuit are repeated here for convenience.

$$\left\{ \begin{array}{l} i_d = i_s = \left( \frac{\mu_F e_i}{r_{ds} + R_D + (1 + \mu_F) R_S} \right) \\ \text{Source DPI} = \left( \frac{r_{ds} + R_D}{(1 + \mu_F)} \right) \\ \text{Drain DPI} = r_{ds} + (1 + \mu_F) R_S \\ \text{Gate DPI} = \infty \end{array} \right\} \quad \text{FET}$$
  

$$\left\{ \begin{array}{l} \text{Collector DPI} = \infty \\ \text{Base DPI} = h_{ie} + (1 + \beta) R_e \\ \text{Emitter DPI} = \left( \frac{h_{ie} + R_B}{1 + \beta} \right) \end{array} \right\} \quad \text{Bipolar Transistor}$$

The amplifier voltage gain  $e_o/e_i$  and output DPI  $O_i$  will be found using the signal circuit shown in Figure 27.

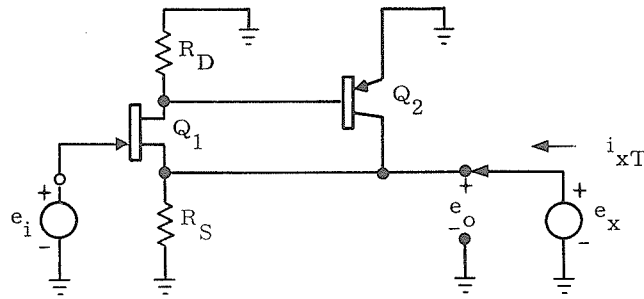


Figure 27. Signal Circuit of Feedback Amplifier

The external source  $e_x$  is applied to the output terminal in order to disable feedback and permit easy analysis of the circuit by conventional DPI methods. The  $i_{xT}$  current is a function of  $e_i$  and  $e_x$  as indicated in Equation (84).

$$i_{xT} = f(e_x, e_i) \quad (84)$$

By applying the superposition theorem, we know that

$$i_{xT} = i_x(e_x = 0, e_i) + i_x(e_x, e_i = 0) \quad (85)$$

and observation will show that

$$i_x(e_x = 0, e_i) = i_{osc} \quad (\text{output short circuit current}) \quad (86)$$

$$i_x(e_x, e_i = 0) = \frac{e_x}{DPI_o} \quad (\text{output DPI}) \quad (87)$$

So

$$i_{xT} = i_{osc} + \frac{e_x}{DPI_o} \quad (88)$$

If we adjust the fictitious  $e_x$  generator so that it is equal to  $e_o$ , then  $i_{xT} = 0$  and Equation (88) becomes

$$0 = i_{osc} + \frac{e_o}{DPI_o} \quad (89)$$

Solving for  $e_o$ , we finally get

$$e_o = -i_{osc} DPI_o \quad (90)$$

In solving for the current  $i_{xT}$  of Equation (85), we obtain both an expression for  $e_o$  and the output DPI. First,  $i_{osc}$  will be found. The circuit of Figure 27 has been redrawn in Figure 28 to clarify the procedure.

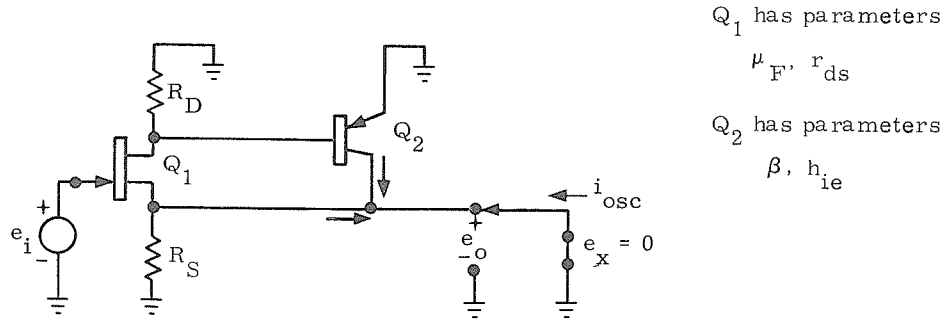


Figure 28. Solving for  $i_{osc}$  in the Feedback Amplifier

$$i_{osc} = - \underbrace{\left( \frac{\mu_F e_i}{r_{ds} + (R_D \parallel h_{ie})} \right)}_{\text{Expression for source and drain current of } Q_1} \left[ 1 + \underbrace{\left( \frac{R_D}{R_D + h_{ie}} \right) \beta}_{\substack{\text{Portion of } i_{osc} \text{ caused by} \\ \text{source current of } Q_1}} \right] \quad (91)$$

Portion of  $i_{osc}$  caused by  $Q_2$  collector current

Second, the portion of the  $i_{xT}$  current caused by the  $e_x$  generator will be determined. The circuit of Figure 27 has been redrawn in Figures 29 and 30 to clarify the procedure.

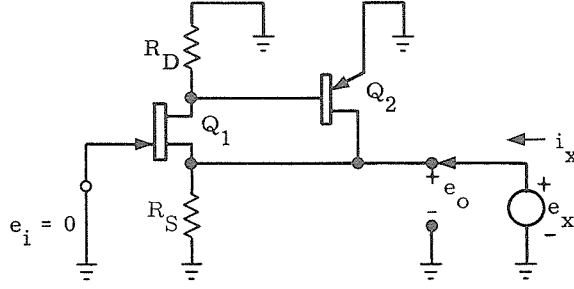


Figure 29. Solving for the Current  $i_x$

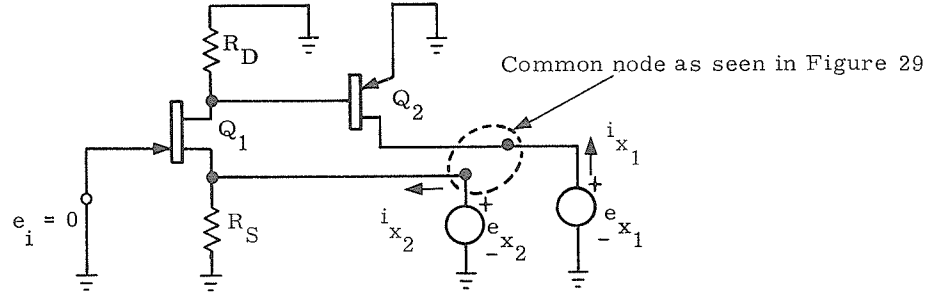


Figure 30. Solving for Current  $i_x$  by Splitting the  $e_x$  Source

$$i_x(e_x) = i_{x1} + i_{x2} \quad \text{when } e_{x1} = e_{x2} = e_x$$

The current  $i_x(e_x)$  is more easily determined by splitting the  $e_x$  generator and using superposition as shown in Figure 30. The total  $i_x(e_x)$  current is found by setting  $e_{x1} = e_{x2} = e_x$  and summing the individual currents.

$$i_x = \left( \frac{e_x}{R_S \parallel \left\{ \frac{r_{ds} + (R_D \parallel h_{ie})}{1 + \mu_F} \right\}} \right) \left[ 1 + \left( \frac{R_S}{R_S + \left\{ \frac{r_{ds} + (R_D \parallel h_{ie})}{1 + \mu_F} \right\}} \right) \left( \frac{R_D}{R_D + h_{ie}} \right) \beta \right] + 0 \quad (92)$$

Observe that we previously determined that  $i_x = \frac{e_x}{DPI_O}$  so that we can now write  $DPI_O$  from inspection of Equation (92).

$$DPI_O = \left\{ \frac{R_S \parallel \left\{ \frac{r_{ds} + (R_D \parallel h_{ie})}{1 + \mu_F} \right\}}{1 + \left( \frac{R_S}{R_S + \left\{ \frac{r_{ds} + (R_D \parallel h_{ie})}{1 + \mu_F} \right\}} \right) \left( \frac{R_D}{R_D + h_{ie}} \right) \beta} \right\} \quad (93)$$

Recall that in the beginning of this problem, the statement was made that the output  $DPI_O$  was not the parallel combination of  $R_S$  and the DPI of the  $Q_1$  source. Equation (93) shows that the output  $DPI_O$  of the amplifier has been reduced due to the feedback, thus confirming the statement.



Using Equation (90) we can now write the complete expression for  $e_o$ .

$$e_o = -i_{osc} DPI_o \quad (90)$$

$$e_o = \underbrace{\left( \frac{\mu_F e_i}{r_{ds} + (R_D \parallel h_{ie})} \right) \left[ 1 + \left( \frac{R_D}{R_D + h_{ie}} \right) \beta \right]}_{-i_{osc}} \underbrace{\left\{ \frac{R_S \parallel \left\{ \frac{r_{ds} + (R_D \parallel h_{ie})}{1 + \mu_F} \right\}}{1 + \left( \frac{R_S}{R_S + \left\{ \frac{r_{ds} + (R_D \parallel h_{ie})}{1 + \mu_F} \right\}} \right) \left( \frac{R_D}{R_D + h_{ie}} \right) \beta} \right\}}_{DPI_o} \quad (94)$$

Dividing both sides of Equation (94) by  $e_i$  yields the desired expression for voltage gain.

If the ideal FET equations (Equations 52A, 53, 54A, 55A) had been used, Equation (94A) would have resulted. Equation (94A) can be obtained by taking the limit as  $r_{ds} \rightarrow \infty$  of Equation (94). Of course, it would be easier to use the ideal FET equations in the first place.

$$e_o = \underbrace{\left( \frac{e_i}{\frac{1}{g_m}} \right) \left[ 1 + \left( \frac{R_D}{R_D + h_{ie}} \right) \beta \right]}_{-i_{osc}} \underbrace{\left\{ \frac{R_S \parallel \left\{ \frac{1}{g_m} \right\}}{1 + \left( \frac{R_S}{R_S + \frac{1}{g_m}} \right) \left( \frac{R_D}{R_D + h_{ie}} \right) \beta} \right\}}_{DPI_o} \quad (94A)$$

As pointed out in previous examples, an explanation of the reasoning process behind the analysis procedure is far more tedious than the procedure itself. A single example is certainly not sufficient to explain all of the subtleties of applying DPI analysis to the solution of feedback circuits, but it does make the reader aware of some of the pitfalls, and this was its purpose.

In order to gain a more thorough insight into the application of DPI analysis, the example problems in Appendix D should be worked and References 6, 7, and 8 should be studied.

## APPENDIX A

### REVIEW OF THEVENIN'S AND NORTON'S THEOREMS

#### Thevenin's Theorem

Thevenin's theorem<sup>4</sup> states that any linear time-invariant oneport network can be replaced by a single voltage source  $V_T$  in series with an impedance  $Z_T$ , and as far as the external terminal conditions are concerned, the Thevenin equivalent circuit cannot be distinguished from the original if  $V_T$  and  $Z_T$  have been properly chosen. This is shown in Figure A1.

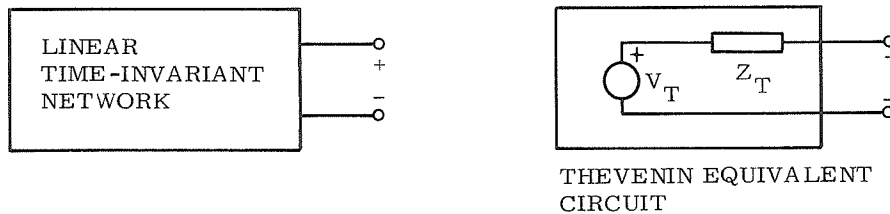


Figure A1. Application of Thevenin's Theorem

A simple procedure for determining the Thevenin equivalent circuit of a linear time-invariant oneport network follows:

1. Remove any networks connected to the oneport.
2. Determine the voltage appearing at the terminals of the oneport by any convenient analysis or measurement technique. This voltage is referred to as the open-circuit or Thevenin voltage  $V_T$ .
3. Replace all independent voltage and current sources by their internal impedances and determine the impedance seen looking into the terminals of the oneport by any convenient analysis or measurement technique. This impedance is referred to as the Thevenin equivalent impedance.
4. Replace the original linear time-invariant oneport with its Thevenin equivalent circuit.

#### Example A1

Determine the Thevenin equivalent circuit of the oneport shown within the dotted lines (Figure A2). Using both the original network and its Thevenin equivalent, determine the voltage across the load resistor  $R_L$  and show that both expressions are the same.

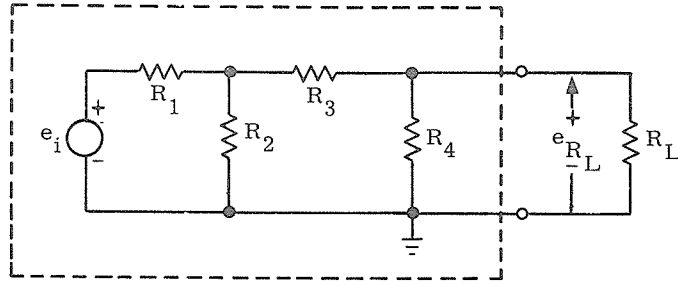


Figure A2. Network Under Consideration

The Thevenin voltage  $V_T$  is found by removing  $R_L$  and computing the voltage appearing across the open circuited terminals as shown in Figure A3.

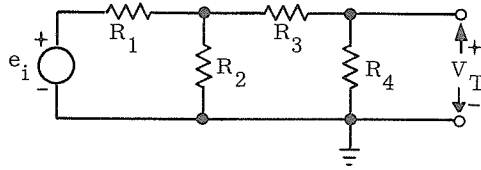


Figure A3. Determination of Thevenin Voltage  $V_T$

$$V_T = e_i \underbrace{\left[ \frac{R_2 \parallel (R_3 + R_4)}{\{R_2 \parallel (R_3 + R_4)\} + R_1} \right]}_{\text{Portion of } e_i \text{ appearing across } R_2} \underbrace{\left[ \frac{R_4}{R_4 + R_3} \right]}_{\text{Portion of voltage across } R_2 \text{ which appears across } R_4} \quad (A1)$$

Voltage divider fractions were used to write Equation (A1) by inspection. This technique is explained in the main body of the report. Any other convenient technique can be applied, but this one is probably the simplest to use.

The Thevenin impedance  $Z_T$  is found by removing  $R_L$  and replacing all independent sources by their internal impedances as shown in Figure A4.

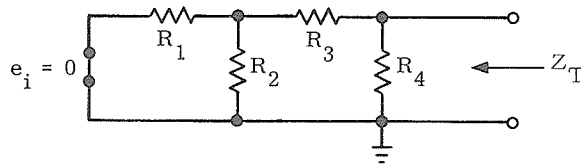


Figure A4. Determination of Thevenin Impedance

$$Z_T = \left\{ R_4 \parallel \left( R_3 + [R_1 + R_2] \right) \right\} \quad (A2)$$

The complete Thevenin equivalent circuit with the load  $R_L$  connected is shown in Figure A5.

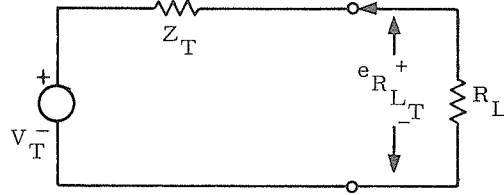


Figure A5. Thevenin Equivalent Circuit of Oneport Shown in Figure A3

Solving for the voltage  $e_{R_{L,T}}$  across  $R_L$  using the Thevenin equivalent circuit of Figure A5, we have Equation (A3).

$$e_{R_{L,T}} = V_T \left[ \frac{R_L}{R_L + Z_T} \right] \quad (A3)$$

Substituting the expressions found for  $V_T$  and  $Z_T$  (Equations A1 and A2) into Equation (A3), we have Equation (A4).

$$e_{R_{L,T}} = e_i \left[ \frac{R_2 \parallel (R_3 + R_4)}{\{R_2 \parallel (R_3 + R_4)\} + R_1} \right] \left[ \frac{R_4}{R_3 + R_4} \right] \left[ \frac{R_L}{R_L + \{R_4 \parallel (R_3 + [R_1 \parallel R_2])\}} \right] \quad (A4)$$

Now, using Figure A2, an expression for  $e_{R_L}$  will be written directly.

$$e_{R_L} = e_i \left[ \frac{\{R_2 \parallel [R_3 + (R_4 \parallel R_L)]\}}{\{R_2 \parallel [R_3 + (R_4 \parallel R_L)]\} + R_1} \right] \left[ \frac{(R_4 \parallel R_L)}{(R_4 \parallel R_L) + R_3} \right] \quad (A5)$$

After simplification, Equations (A4) and (A5) can be shown to be identical, indicating that the Thevenin equivalent circuit has the same terminal characteristics as the original circuit. Another way to check and see if Equations (A4) and (A5) produce the same answer is to choose some convenient values for the circuit components and sources. If all R's are chosen to be  $1\Omega$  and  $e_i = 8$  volts,  $e_{R_L}$  and  $e_{R_{L,T}}$  will be found to be 1 volt.

## Norton's Theorem

Norton's theorem<sup>5</sup> is the dual of Thevenin's theorem, and states that any linear time-invariant oneport network can be replaced by a single current source  $i_N$  in shunt with an impedance  $Z_N$ , and as far as the external terminal conditions are concerned, the Norton equivalent circuit cannot be distinguished from the original oneport if  $i_N$  and  $Z_N$  are chosen properly. This is shown in Figure A6.

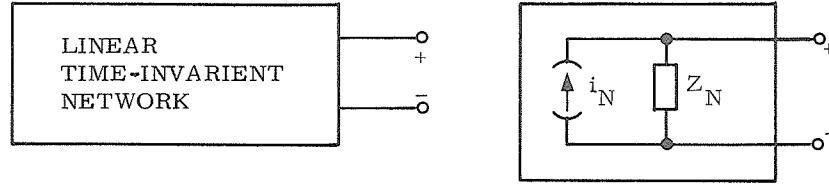


Figure A6. Application of Norton's Theorem

A simple procedure for determining the Norton equivalent circuit of a linear time-invariant oneport follows:

1. Remove any networks connected to the oneport.
2. Short the terminals of the oneport and determine the short-circuit current that flows by any convenient analysis or measurement technique. This current is referred to as the Norton current  $i_N$ .
3. Replace all independent sources by their internal impedances and determine the impedance seen looking into the terminals of the oneport by any convenient analysis or measurement technique. This impedance is referred as the Norton impedance  $Z_N$ .
4. Replace the original linear time-invariant oneport with its Norton equivalent circuit.

#### Example A2

Using the Thevenin equivalent circuit found in Example A1 (Figure A5), determine its Norton equivalent circuit and then solve for  $e_{R_{L_N}}$  using the Norton equivalent circuit and show that the answer is the same as given by Equation (A4).

The Norton current  $i_N$  is found by removing  $R_L$  and computing the current flowing through the short as shown in Figure A7.

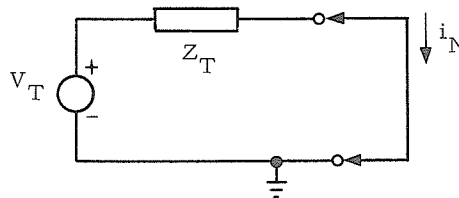


Figure A7. Determination of Norton Current

$$i_N = \frac{V_T}{Z_T} \quad (A6)$$

The Norton impedance  $Z_N$  is found by removing  $R_L$ , replacing  $V_T$  by its internal impedance (short circuit), and measuring the impedance seen looking into the oneport terminals as shown in Figure A8.

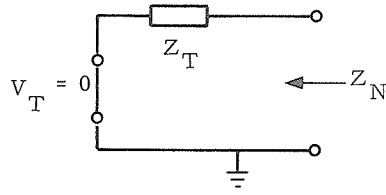


Figure A8. Determination of Norton Impedance

$$Z_N = Z_T$$

The complete Norton equivalent circuit is shown in Figure A9 with the load connected.

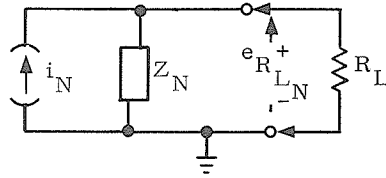


Figure A9. Norton Equivalent Circuit of Figure A5

$$e_{R_{L_N}} = i_N \left( \frac{Z_N}{Z_N + R_L} \right) R_L \quad (A7)$$

$$e_{R_{L_N}} = \frac{V_T}{Z_T} \left( \frac{Z_T}{Z_T + R_L} \right) R_L = V_T \left( \frac{R_L}{Z_T + R_L} \right) \quad (A8)$$

Note that Equation A8 is identical to Equation (A3), indicating that the Norton and Thevenin equivalent circuits have the same terminal characteristics.

## APPENDIX B

### DETERMINATION OF SIGNAL CURRENT DIRECTIONS IN ACTIVE DEVICES OPERATING IN THEIR LINEAR REGIONS

This appendix discusses the procedures and reasoning used in determining the directions of signal current flow in active devices operating in their linear regions. Current flow through a transistor or vacuum tube is unidirectional, and application of a signal to the control electrode causes the magnitude of this current flow to increase or decrease. Unfortunately, from a pedagogical standpoint, thinking of the signal as causing an increase or decrease in the magnitude but not a change in direction of the total current flowing through the active device frequently leads to confusion when one attempts to determine phase relationships within the circuit. The direction of quiescent current flow is, of course, dependent upon the device being used, e.g., current flows from the collector and base to the emitter in an NPN transistor as shown in Figure B1.

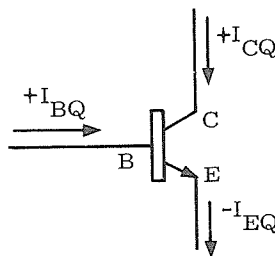


Figure B1. Quiescent Currents of an NPN Transistor  
Operating in its Active Region

Current flow into the terminal of a device is treated as a positive current, and current flowing out of the terminal of a device is treated as a negative current. Although this is the conventional way of treating current directions, it is not necessary to follow it as long as some consistent procedure is utilized.

In a PNP transistor, all of the current directions are exactly opposite to those of the NPN device. Current flow is from the drain to source in an N-channel FET, and is just the opposite in a P-channel FET. The current flow in vacuum tubes is always from plate to cathode. These facts are, of course, well known to anyone familiar with these devices.

Consider the effect of applying a signal current to the base of the NPN transistor shown in Figure B1. The signal current will algebraically add to the quiescent base current  $I_{BQ}$  in such a way as to increase or decrease the total base current, thus causing the absolute magnitudes of the total collector and emitter currents to increase or decrease correspondingly. It is important to realize that the total base, emitter and collector currents of a transistor are each composed of two parts. The first part is the quiescent terminal current, and the second part is the current

caused by the signal. The direction in which the quiescent terminal currents flow is strictly dependent upon the active device being utilized; this is shown in Equations (B1) through (B6) where Equations (B1), (B2), and (B3) are for an NPN transistor and Equations (B4), (B5), and (B6) are for a PNP transistor.

$$\begin{array}{lcl}
 \text{For} & \left\{ \begin{array}{l} |i_{BT}| = |I_{BQ}| \pm |i_{bs}| \\ |i_{CT}| = |I_{CQ}| \pm |i_{cs}| \\ - |i_{ET}| = -|I_{EQ}| \mp |i_{es}| \end{array} \right\} & \begin{array}{l} \text{(B1)} \\ \text{(B2)} \\ \text{(B3)} \end{array} \\
 \text{NPN} & & \\
 \text{Transistor} & & \\
 \\
 \text{For} & \left\{ \begin{array}{l} - |i_{BT}| = -|I_{BQ}| \pm |i_{bs}| \\ - |i_{CT}| = -|I_{CQ}| \pm |i_{cs}| \\ |i_{ET}| = |I_{EQ}| \mp |i_{es}| \end{array} \right\} & \begin{array}{l} \text{(B4)} \\ \text{(B5)} \\ \text{(B6)} \end{array} \\
 \text{PNP} & & \\
 \text{Transistor} & & 
 \end{array}$$

The subscripts T, Q, and S stand for total, quiescent, and signal respectively.

Note especially the ordering of the algebraic signs used on the signal currents for both the NPN and PNP transistors. Two things should become apparent. First, the polarities of the signal base and collector currents are always the same but opposite from the emitter signal current. Second, the signal current polarities are the same for both NPN and PNP transistors, although the polarities for the quiescent and total currents are reversed. This second observation is especially important because it means that we can ignore whether a transistor is an NPN or a PNP device when performing a signal circuit analysis. Note especially that for linear operation of the transistor to be maintained, it is necessary to keep the absolute magnitude of the signal currents less than the absolute magnitude of the quiescent currents.

When analyzing a linear circuit containing active devices, the analysis is generally performed in two distinct steps. First, the dc or quiescent circuit is analyzed by replacing all of the signal sources by their internal impedances. Second, the ac or signal circuit is solved by replacing all of the dc sources by their internal impedances. (The dc sources are usually considered as signal short circuits.) Errors are most likely to occur when the signal analysis of the circuit is performed. These errors usually occur because the analyst does not completely separate the dc from the ac analysis, e. g., when considering the base current caused by a signal, he considers  $i_{BT}$  instead of  $i_{bs}$ . A positive going signal voltage applied to the grid of a vacuum tube or to the gate of an FET will cause a signal current to flow into the plate or drain terminal and out of the cathode or source terminal respectively; likewise, a negative going signal voltage applied to the grid of a vacuum tube or to the gate of an FET will cause a signal current to flow out of the plate or drain terminal and into the cathode or source terminal respectively. In the case of a triode vacuum tube, the plate and cathode currents have the same absolute magnitude; the drain and source currents of an FET also have the same absolute magnitude. These concepts are demonstrated in Figures B2 through B6.



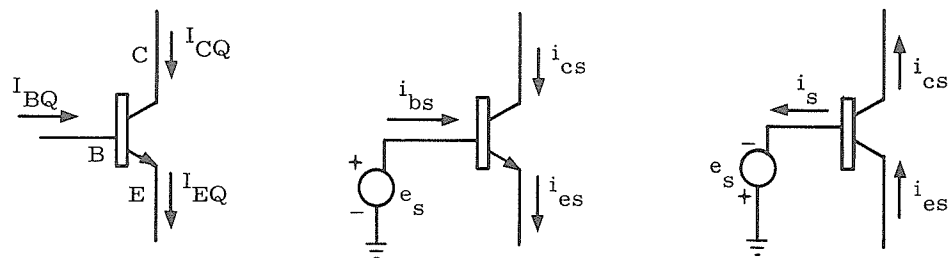


Figure B2. Quiescent and Signal Currents in the NPN Transistor

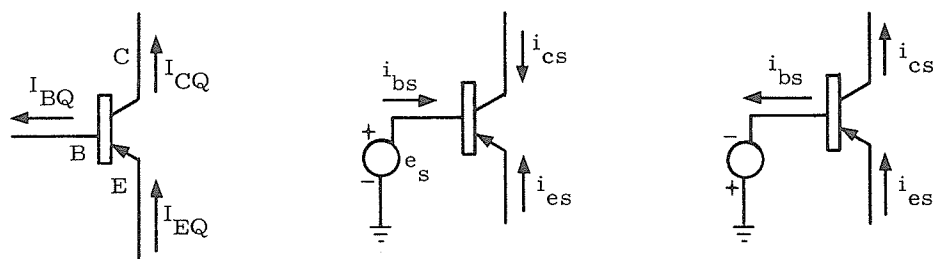


Figure B3. Quiescent and Signal Currents in the PNP Transistor

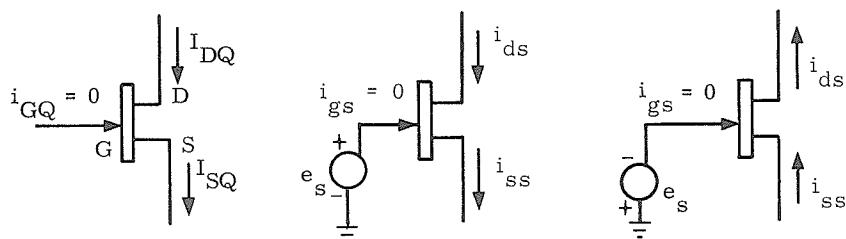


Figure B4. Quiescent and Signal Currents in the N-Channel FET

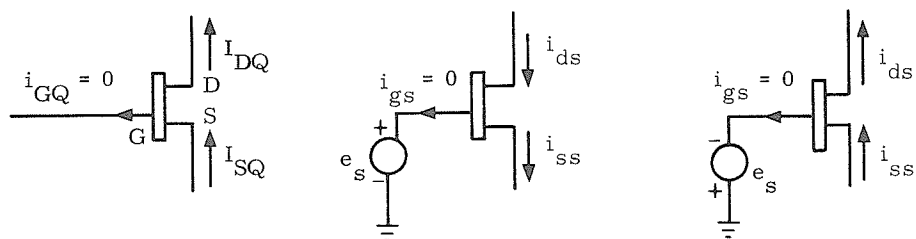


Figure B5. Quiescent and Signal Currents in the P-Channel FET

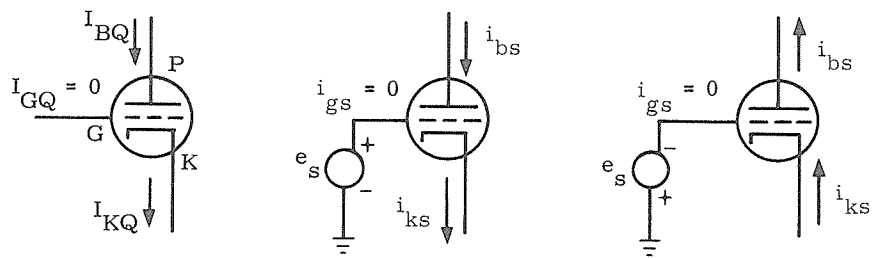


Figure B6. Quiescent and Signal Currents in the Triode Vacuum Tube

## APPENDIX C

### DPI ANALYSIS USING THE LAPLACE TRANSFORM METHOD

In this appendix we demonstrate how DPI analysis can be used in conjunction with the Laplace transform to obtain the transient response of a circuit containing active devices. The assumption is made that the reader is familiar with the application of the Laplace transform to circuit solutions. Assumptions made about the circuits to be analyzed are:

1. The simplified models used to derive the DPI equations still hold.
2. The input signal or signals do not drive the active device or devices into their nonlinear region or regions.

#### Example C1

Problem-- Determine the response of the single stage amplifier shown in Figure C1 when  $e_i(t) = u(t)$  where  $u(t)$  is a unit step applied at  $t = 0$ .

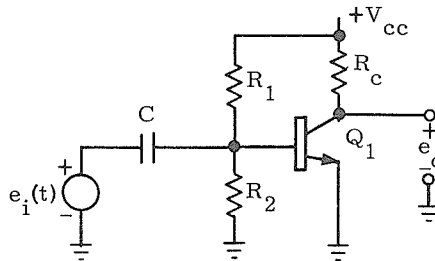


Figure C1. Single Stage Transistor Amplifier

Solution--The transformed signal circuit is shown in Figure C2.

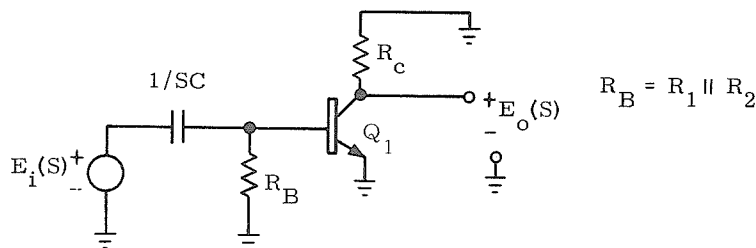


Figure C2. Transformed Amplifier Circuit

Using DPI analysis, the expression for  $E_o(s)$  can be written in a single step and is shown in Equation (C1).

$$E_o(S) = - \left[ \frac{E_i(S)}{1/SC + (R_B \parallel h_{ie})} \right] \left[ \frac{R_B}{R_B + h_{ie}} \right] \beta R_c \quad (C1)$$

Now, Equation (C1) will be manipulated into a form which will eventually permit the inverse transform to be taken. We are interested in obtaining the forward voltage transfer function  $H(S) = \frac{E_o(S)}{E_i(S)}$ .

$$\frac{E_o(S)}{E_i(S)} = H(S) = - \left[ \frac{SC}{1 + SC(R_B \parallel h_{ie})} \right] \left[ \frac{R_B}{R_B + h_{ie}} \right] \beta R_c \quad (C2)$$

Placing Equation (C2) into standard form, we have Equation (C3):

$$H(S) = - \left[ \frac{S}{S + \left\{ \frac{1}{C(R_B \parallel h_{ie})} \right\}} \right] \left[ \frac{R_B}{R_B + h_{ie}} \right] \beta R_c \left[ \frac{1}{R_B \parallel h_{ie}} \right] \quad (C3)$$

Let

$$\left\{ \frac{1}{C(R_B \parallel h_{ie})} \right\} = K_1$$

and

$$\left[ \frac{R_B}{R_B + h_{ie}} \right] \beta R_c \left[ \frac{1}{R_B \parallel h_{ie}} \right] = K_2$$

Then

$$H(S) = - \left( \frac{K_2 S}{S + K_1} \right) \quad (C4)$$

We know that

$$E_o(S) = H(S)E_i(S). \quad (C5)$$

The Laplace transform of a unit step input voltage applied at  $t = 0$  is given in Equation (C6).

$$\mathcal{L}(u(t)) = \frac{1}{S} \quad (C6)$$

Placing the values of  $H(S)$  and  $E_i(S)$  into Equation (C5) and taking the inverse Laplace transform gives the output as a function of time.

$$\begin{aligned} E_o(S) &= - \left( \frac{K_2 S}{S + K_1} \right) \left( \frac{1}{S} \right) = - \left( \frac{K_2}{S + K_1} \right) \\ e_o(t) &= \mathcal{L}^{-1}(E_o(S)) = -K_2 e^{-K_1 t} \\ e_o(t) &= -K_2 e^{-K_1 t} \end{aligned} \quad (C7)$$

Equation (C7) indicates that the response of the amplifier to a unit voltage step on the input is a decaying exponential with a time constant  $K_1$  and a maximum amplitude  $K_2$ .

### Example C2

Problem--Determine the response of the single stage amplifier shown in Figure C3 when  $e_i(t) = u(t)$ , where  $u(t)$  is a unit step of voltage applied at  $t = 0$ . Assume linear operation.

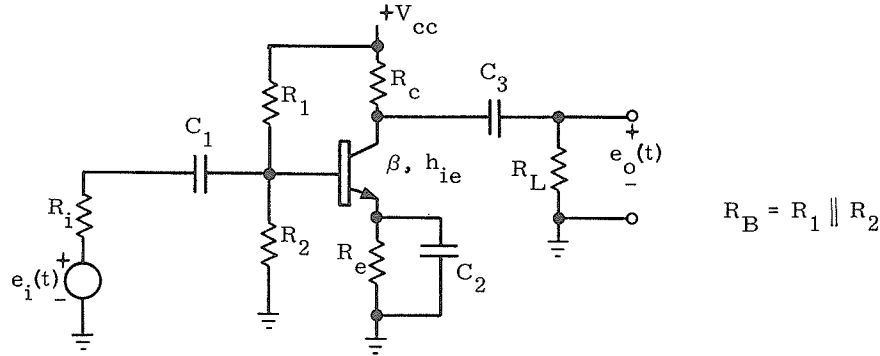


Figure C3. Circuit for Example C2

Solution--Using the Laplace transform and DPI analysis, an expression for  $E_o(S)$  can be written by inspection.

$$E_o(S) = \left[ \frac{-E_i(S)}{R_i + \frac{1}{SC_1} + \left\{ R_B \parallel \left[ h_{ie} + (1 + \beta) \left( R_e \parallel \frac{1}{SC_2} \right) \right] \right\}} \right] \cdot \left[ \frac{R_B}{R_B + \left[ h_{ie} + (1 + \beta) \left( R_e \parallel \frac{1}{SC_2} \right) \right]} \right] \cdot \left[ \frac{\beta R_c}{R_c + \left( \frac{1}{SC_3} + R_L \right)} \right] R_L \quad (C8)$$

$$\mathcal{L}(u(t)) = \frac{1}{S} \quad (C9)$$

Substituting Equation (C9) into (C8) we have

$$E_o(S) = \left( \frac{1}{S} \right) \left[ \frac{-1}{R_i + \frac{1}{SC_1} + \left\{ R_B \parallel \left[ h_{ie} + (1 + \beta) \left( R_e \parallel \frac{1}{SC_2} \right) \right] \right\}} \right] \left[ \frac{R_B}{R_B + \left[ h_{ie} + (1 + \beta) \left( R_e \parallel \frac{1}{SC_2} \right) \right]} \right] \beta \left[ \frac{R_c}{R_c + \left( \frac{1}{SC_3} + R_L \right)} \right] R_L \quad (C10)$$

The algebraic manipulation of Equation (C10) into the proper form for obtaining the inverse Laplace transform is tedious if done using symbols. It is far simpler to solve Equation (C10) when the parameter values are substituted into the equation.

$$e_o(t) = \mathcal{L}^{-1}\left(E_o(s)\right) \quad (C11)$$

## APPENDIX D

### ADDITIONAL EXAMPLES OF THE APPLICATION OF DPI ANALYSIS

This appendix presents a sampling of circuit problems and the solutions obtained by applying DPI analysis. In all of the following example problems it is assumed that we are operating in the linear regions of the active devices.

#### Example D1

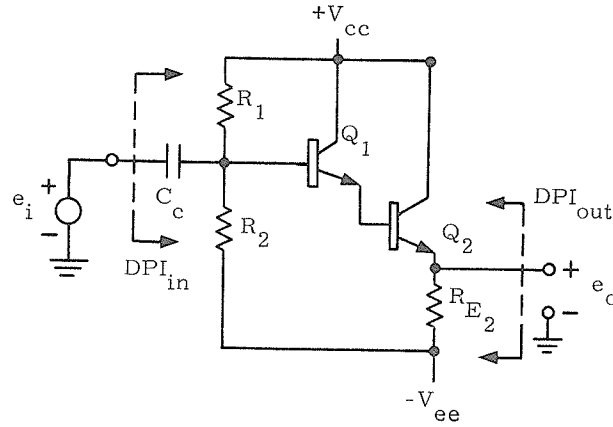


Figure D1. Darlington Circuit

Problem--Find the mid-band voltage gain  $e_o/e_i$ ,  $DPI_{in}$  and  $DPI_{out}$  using DPI analysis. The answers should be written in a single step.

Solution--

$$DPI_{in} = (R_1 \parallel R_2) \parallel \left\{ h_{ie1} + (1 + \beta_1) \left[ h_{ie2} + (1 + \beta_2) R_{E2} \right] \right\} \quad (D1)$$

$$DPI_{out} = R_{E2} \parallel \left\{ \frac{h_{ie2} + \left[ \frac{h_{ie1}}{(1 + \beta_1)} \right]}{(1 + \beta_2)} \right\} \quad (D2)$$

$$e_o = \left\{ \frac{e_i}{(R_1 \parallel R_2) \parallel \left\{ h_{ie1} + (1 + \beta_1) \left[ h_{ie2} + (1 + \beta_2) R_{E2} \right] \right\}} \right\} \cdot \left\{ \frac{(R_1 \parallel R_2)}{\left\{ h_{ie1} + (1 + \beta_1) \left[ h_{ie2} + (1 + \beta_2) R_{E2} \right] \right\} + (R_1 \parallel R_2)} \right\} (1 + \beta_1) (1 + \beta_2) R_{E2} \quad (D3)$$

Example D2

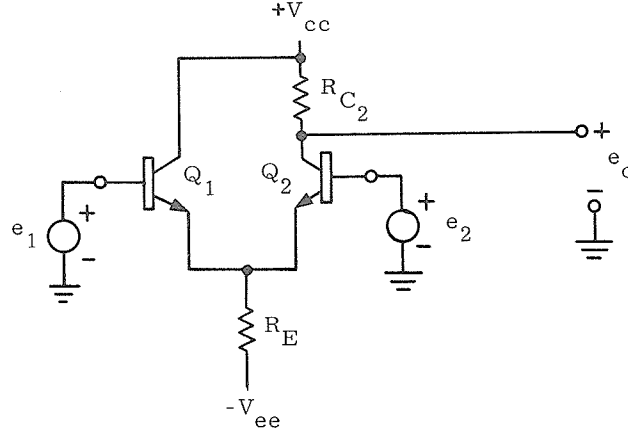


Figure D2. Emitter-Coupled Differential Amplifier

Problem--Using DPI analysis, write an expression for  $e_o$  as a function of  $e_1$  and  $e_2$  and explain why this is a poor differential amplifier even if the transistor parameters are identical.

Solution--

$$e_o = \left\{ \frac{e_1}{h_{ie_1} + (1 + \beta_1) \left[ R_E \parallel \left( \frac{h_{ie_2}}{1 + \beta_2} \right) \right]} \right\} (1 + \beta_1) \left[ \frac{R_E}{R_E + \left( \frac{h_{ie_2}}{1 + \beta_2} \right)} \right] \left( \frac{\beta_2}{1 + \beta_2} \right) R_{C_2} - \left\{ \frac{e_2}{h_{ie_2} + (1 + \beta_2) \left[ R_E \parallel \left( \frac{h_{ie_1}}{1 + \beta_1} \right) \right]} \right\} (\beta_2) R_{C_2} \quad (D4)$$

Now, if we assume  $h_{ie_1} = h_{ie_2} = h_{ie}$  and  $\beta_1 = \beta_2 = \beta$ , we can rewrite Equation (D4) as shown in Equation (D5).

$$e_o = \left\{ \frac{e_1}{h_{ie} + (1 + \beta) \left[ R_E \parallel \left( \frac{h_{ie}}{1 + \beta} \right) \right]} \right\} \left[ \frac{R_E}{R_E + \frac{h_{ie}}{1 + \beta}} \right] \beta R_{C_2} - \left\{ \frac{e_2}{h_{ie} + (1 + \beta) \left[ R_E \parallel \left( \frac{h_{ie}}{1 + \beta} \right) \right]} \right\} \beta R_{C_2} \quad (D5)$$

Removing common terms from Equation (D5) yields Equation (D6)

$$e_o = \left( e_1 \left[ \frac{R_E}{R_E + \left( \frac{h_{ie}}{1 + \beta} \right)} \right] - e_2 \right) \left\{ \frac{\beta R_{C_2}}{h_{ie} + (1 + \beta) \left[ R_E \parallel \left( \frac{h_{ie}}{1 + \beta} \right) \right]} \right\} \quad (D6)$$



Equation (D6) clearly demonstrates why the circuit shown in Figure D2 is a poor differential amplifier. The term multiplying  $e_1$  will not permit  $e_o$  to go to zero when  $e_1 = e_2$ , i.e., the amplifier has a poor common-mode rejection.

#### Example D3

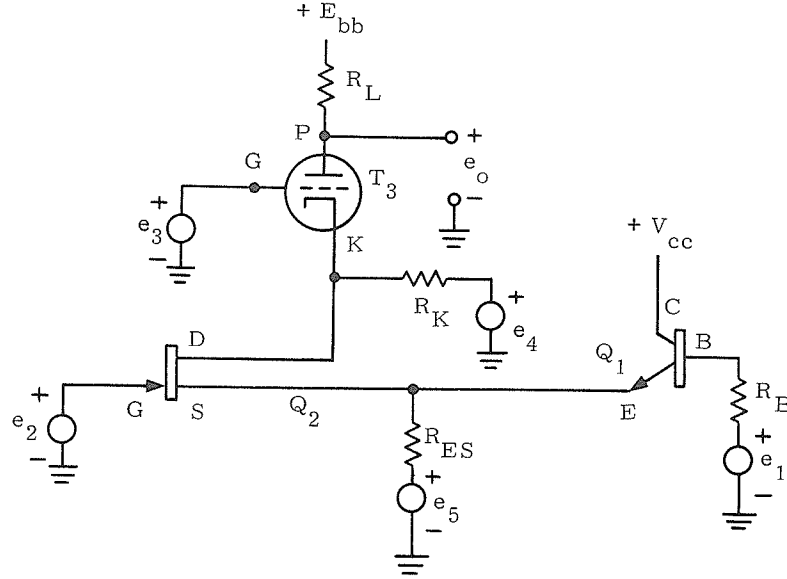


Figure D3. Circuit Using a Vacuum Tube, Ideal FET, and Transistor

Problem--Determine  $e_o$  by using DPI analysis and the superposition theorem. Write the solution in a single step.

Solution--

$$\begin{aligned}
 e_o = & \left\{ \frac{e_1}{R_B + h_{ie} + (1 + \beta) \left[ R_{ES} \parallel \frac{1}{g_{m2}} \right]} \right\} (1 + \beta) \left\{ \frac{R_{ES}}{R_{ES} + \frac{1}{g_{m2}}} \right\} \left\{ \frac{R_K}{R_K + \left( \frac{r_p + R_L}{1 + \mu_3} \right)} \right\} R_L \\
 & - \left\{ \frac{e_2}{\frac{1}{g_{m2}} + \left\{ R_{ES} \parallel \left( \frac{h_{ie} + R_B}{1 + \beta} \right) \right\}} \right\} \left\{ \frac{R_K}{R_K + \left( \frac{r_p + R_L}{1 + \mu_3} \right)} \right\} R_L - \left\{ \frac{\mu e_3}{r_p + R_L + (1 + \mu_3) R_K} \right\} R_L \\
 & + \left\{ \frac{e_4}{R_K + \left( \frac{r_p + R_L}{1 + \mu_3} \right)} \right\} R_L \\
 & + \left\{ \frac{e_5}{R_{ES} + \left\{ \left( \frac{h_{ie} + R_B}{1 + \beta} \right) \parallel \left( \frac{1}{g_{m2}} \right) \right\}} \right\} \left\{ \frac{\left( \frac{h_{ie} + R_B}{1 + \beta} \right)}{\left( \frac{h_{ie} + R_B}{1 + \beta} \right) + \left( \frac{1}{g_{m2}} \right)} \right\} \left\{ \frac{R_K}{R_K + \left( \frac{r_p + R_L}{1 + \mu_3} \right)} \right\} R_L
 \end{aligned} \tag{D7}$$

### Example D4

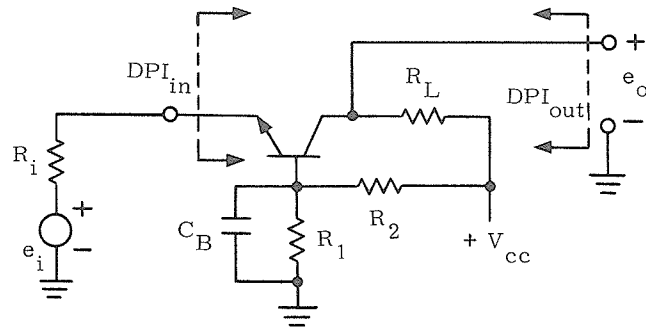


Figure D4. Common-Base Amplifier

Problem--Determine the mid-band voltage gain, the  $DPI_{in}$ , and the  $DPI_{out}$  using DPI analysis.  
Write each answer in a single step.

Solution--

$$DPI_{in} = \left( \frac{h_{ie}}{1 + \beta} \right) \quad (D8)$$

$$DPI_{out} = R_L \quad (D9)$$

$$e_o = \left\{ \frac{e_i}{R_i + \left( \frac{h_{ie}}{1 + \beta} \right)} \right\} \left( \frac{\beta}{1 + \beta} \right) R_L \quad (D10)$$

It is interesting to note how low the input impedance is if we assume some typical values for the circuit parameters

Let

$$I_{EQ} = 1 \text{ ma}, \quad \beta = 100$$

$$h_{ie} = \frac{26 \times 10^{-3} (1 + \beta)}{I_{EQ}} \cong 2600 \Omega \quad (\text{From Equation (31) in text})$$

$$DPI_{in} = \frac{h_{ie}}{1 + \beta} \cong 26 \Omega$$

Example D5

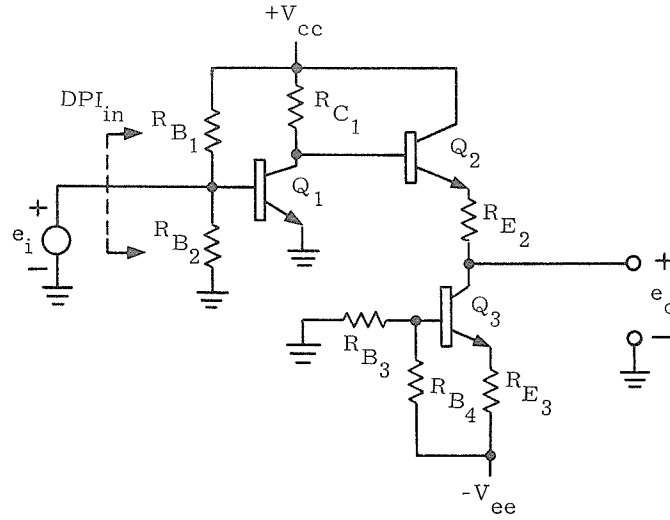


Figure D5. Level Shifting Cascode Amplifier

Problem--Determine the voltage gain,  $DPI_{in}$  and  $DPI_{out}$  using DPI analysis.

Solution--

$$DPI_{in} = \left\{ \left( R_{B1} \parallel R_{B2} \right) \parallel \left( h_{ie1} \right) \right\} \quad (D11)$$

$$DPI_{out} = R_{E2} + \left( \frac{h_{ie2} + R_{C1}}{1 + \beta_2} \right) \quad (D12)$$

$$e_o = \left\{ \frac{-e_i}{\left( R_{B1} \parallel R_{B2} \right) \parallel h_{ie1}} \right\} \left\{ \frac{R_{B1} \parallel R_{B2}}{\left( R_{B1} \parallel R_{B2} \right) + h_{ie1}} \right\} \beta_1 R_{C1} \quad (D13)$$

This circuit is interesting from the standpoint that the signal voltage appearing at the collector of  $Q_1$  is almost the same as the signal voltage appearing at the collector of  $Q_3$ . No signal current flows in the base or emitter of  $Q_2$  because  $DPI_{Base\ 2} \approx \infty$ .

$$DPI_{Base\ 2} = h_{ie2} + (1 + \beta_2) \left[ R_{E2} + \infty \right] = \infty. \quad (D14)$$

### Example D6

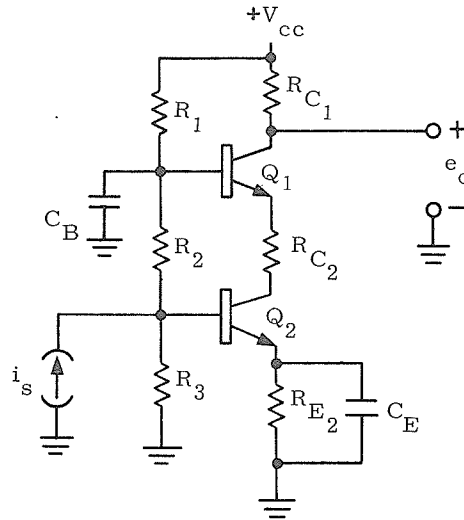


Figure D6. Cascode Amplifier

Problem--Determine  $e_o$  using DPI analysis. Assume  $C_B$  and  $C_E$  appear as signal short circuits.

Solution--

$$e_o = -i_s \left[ \frac{(R_2 \parallel R_3)}{(R_2 \parallel R_3) + h_{ie2}} \right] (\beta_2) \left( \frac{\beta_1}{1 + \beta_1} \right) R_{C1} \quad (D15)$$

### Example D7

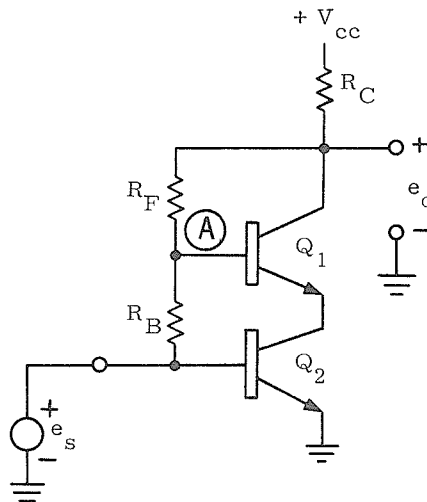
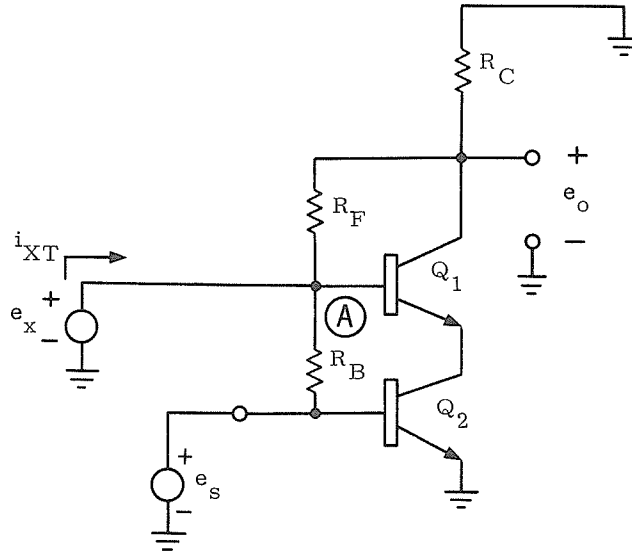


Figure D7. Two-Transistor Feedback Circuit

Problem--Determine  $e_o$ ,  $DPI_{in}$  and  $DPI_{out}$  using DPI analysis.

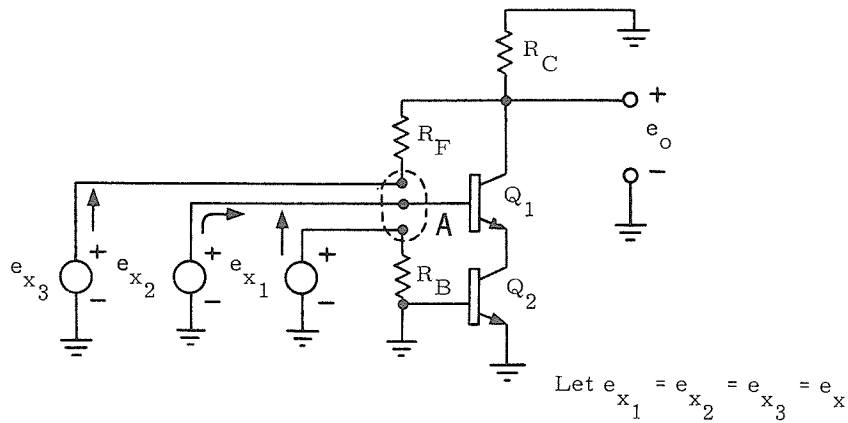
Solution--The form of solution presented herein is only one of several that can be obtained depending upon how the problem is attacked.

In order to analyze this circuit, feedback will be disabled by applying a fictitious generator to point A,



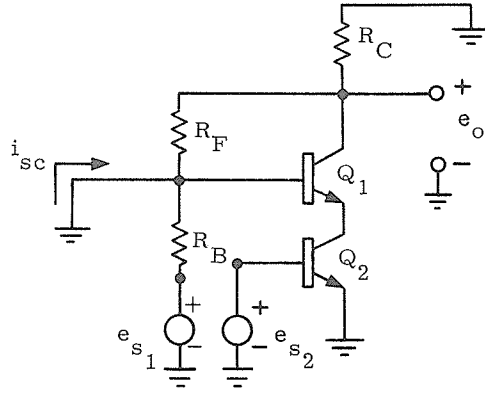
where  $i_{XT} = f(e_x, e_s = 0) + f(e_x = 0, e_s)$  by superposition.

First, the portion of  $i_{XT}$  due to  $e_x$  acting alone will be determined.



$$i_{XT} \text{ (due to } e_x) = \frac{e_{x1}}{R_B} + 0 + \frac{e_{x3}}{R_F + R_C} = e_x \left( \frac{1}{R_B} + \frac{1}{R_F + R_C} \right) \quad (D16)$$

Second, the portion of  $i_{XT}$  due to  $e_s$  acting alone will be determined.



$$\text{Let } e_{s_1} = e_{s_2} = e_s$$

$$i_{XT} (\text{due to } e_s) = i_{sc} = \left( \frac{-e_{s_1}}{R_B} + \left( \frac{e_{s_2}}{h_{ie_2}} \right) \beta_2 \left[ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right] \right)$$

$$i_{sc} = -e_s \left[ \frac{1}{R_B} - \left( \frac{\beta_2}{h_{ie_2}} \right) \left\{ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right\} \right] \quad (D17)$$

$$i_{XT} = e_x \left( \frac{1}{R_B} + \frac{1}{R_F + R_C} \right) - e_s \left[ \frac{1}{R_B} - \left( \frac{\beta_2}{h_{ie_2}} \right) \left\{ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right\} \right] \quad (D18)$$

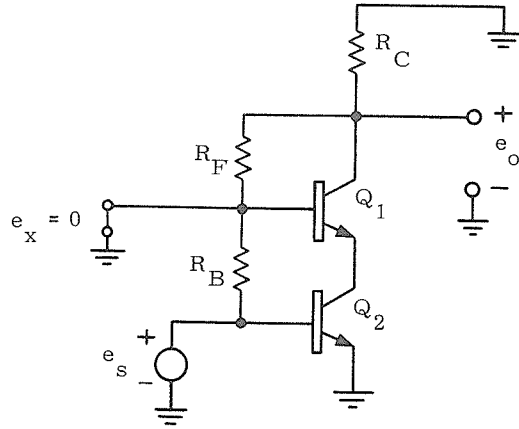
The  $e_x$  generator is now forced to be equal to the voltage at point A by setting  $i_{XT} = 0$ .

Solving for the voltage at point A from Equation (D18) we have

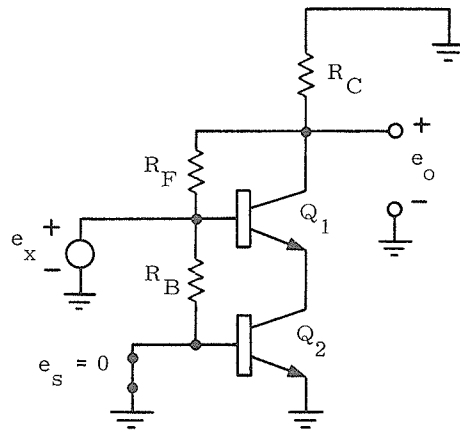
$$e_x = e_A = \frac{e_s \left[ \frac{1}{R_B} - \left( \frac{\beta_2}{h_{ie_2}} \right) \left\{ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right\} \right]}{\left( \frac{1}{R_B} + \frac{1}{R_F + R_C} \right)} \quad (D19)$$

Now, let us solve for  $e_o$  as a function of  $e_x$  and  $e_s$  by applying superposition, i. e.,

$$e_o = f(e_x, e_s = 0) + f(e_x = 0, e_s) \quad .$$



$$e_o \text{ (due to } e_s) = \left( \frac{-e_s}{h_{ie2}} \right) \beta_2 \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_F}{R_F + R_C} \right) R_C$$



$$e_o \text{ (due to } e_x) = e_x \left[ \frac{R_C}{R_C + R_F} \right]$$

Therefore, the total expression for  $e_o$  is

$$e_o = \left( \frac{-e_s}{h_{ie2}} \right) \beta_2 \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_F}{R_F + R_C} \right) R_C + e_x \left( \frac{R_C}{R_C + R_F} \right) \quad (D20)$$

Substituting Equation (D19) into Equation (D20) produces the complete expression for  $e_o = f(e_s)$ , as shown in Equation (D21).

$$e_o = -e_s \left\{ \left( \frac{\beta_2}{h_{ie2}} \right) \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_F}{R_F + R_C} \right) R_C - \left( \frac{R_C}{R_C + R_F} \right) \left[ \frac{\frac{1}{R_B} - \left( \frac{\beta_2}{h_{ie2}} \right) \left\{ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right\}}{\frac{1}{R_B} + \frac{1}{R_F + R_C}} \right] \right\} \quad (D21)$$

The  $DPI_{in}$  can be found by solving for the total signal current flowing from the  $e_s$  source when  $e_x = e_A$ .

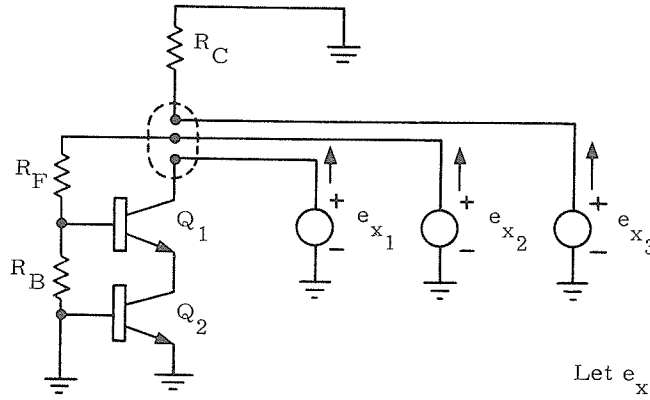
$$i_{ST} = \left( \frac{e_s}{h_{ie_2}} \right) + \left( \frac{e_s - e_A}{R_B} \right) \quad (D22)$$

Substituting the expression for  $e_A$  into Equation (D22) yields

$$i_{ST} = e_s \left( \frac{1}{h_{ie_2}} + \frac{1}{R_B} - \frac{1}{R_B} \left[ \frac{\frac{1}{R_B} - \left( \frac{\beta_2}{h_{ie_2}} \right) \left\{ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right\}}{\frac{1}{R_B} + \frac{1}{R_F + R_C}} \right] \right)$$

$$DPI_{in} = \frac{e_s}{i_{ST}} = \left( h_{ie_2} \right) \parallel \left( R_B \right) \parallel \left\{ \frac{\left( 1 + \frac{R_B}{R_F + R_C} \right)}{-\frac{1}{R_B} + \left( \frac{\beta_2}{h_{ie_2}} \right) \left\{ \left( \frac{1}{1 + \beta_1} \right) + \left( \frac{\beta_1}{1 + \beta_1} \right) \left( \frac{R_C}{R_C + R_F} \right) \right\}} \right\} \quad (D23)$$

The  $DPI_{out}$  can be found in several ways but the simplest is probably to apply an external generator to the  $e_o$  terminal and solve for the current. Using this technique, the  $DPI_{out}$  is given in Equation (D24).



$$i_{XT} \text{ (due to } e_x) = 0 + \left( \frac{e_{x2}}{R_F + R_B} \right) + \left( \frac{e_{x3}}{R_C} \right) = e_x \left( \frac{1}{R_C} + \frac{1}{R_F + R_B} \right)$$

$$\frac{e_x}{i_{XT}} = DPI_{out} = (R_F + R_B) \parallel (R_C) \quad (D24)$$



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